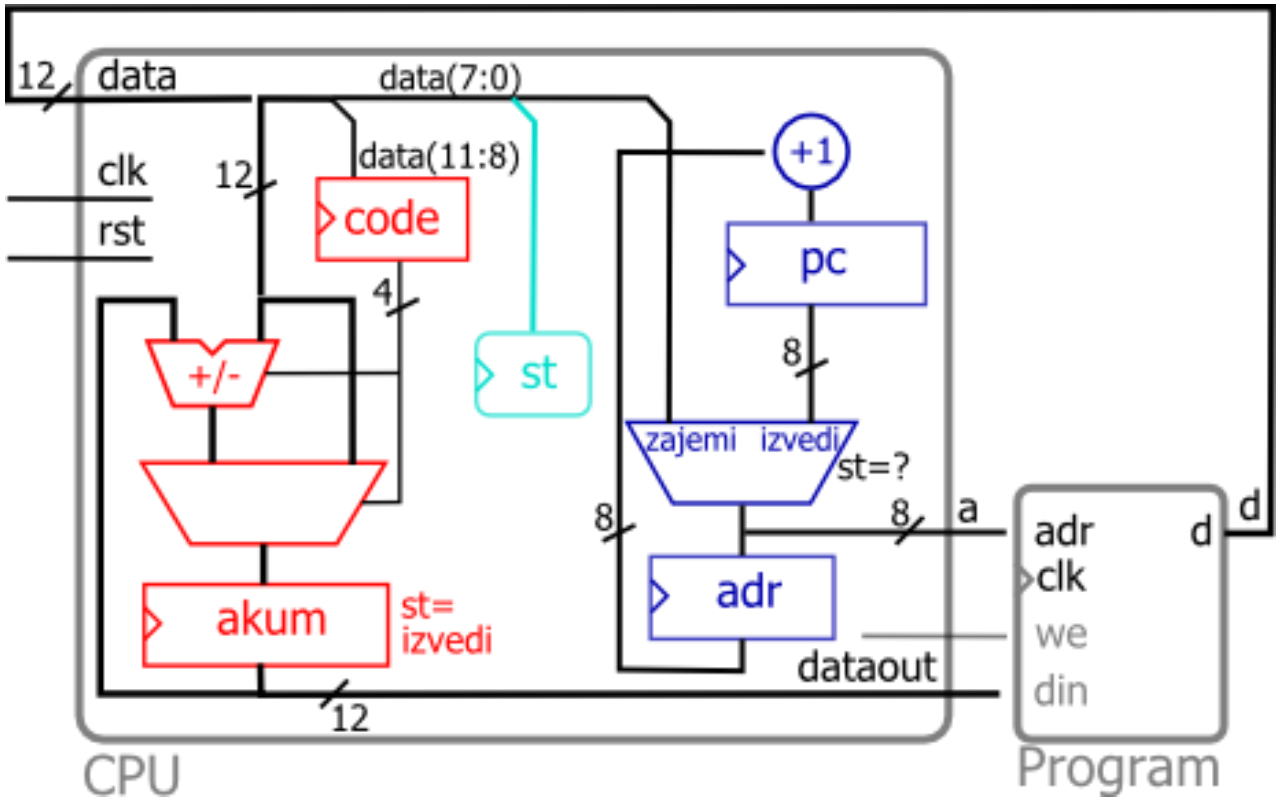
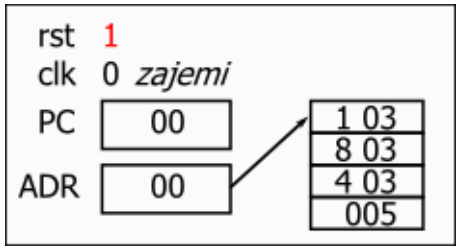
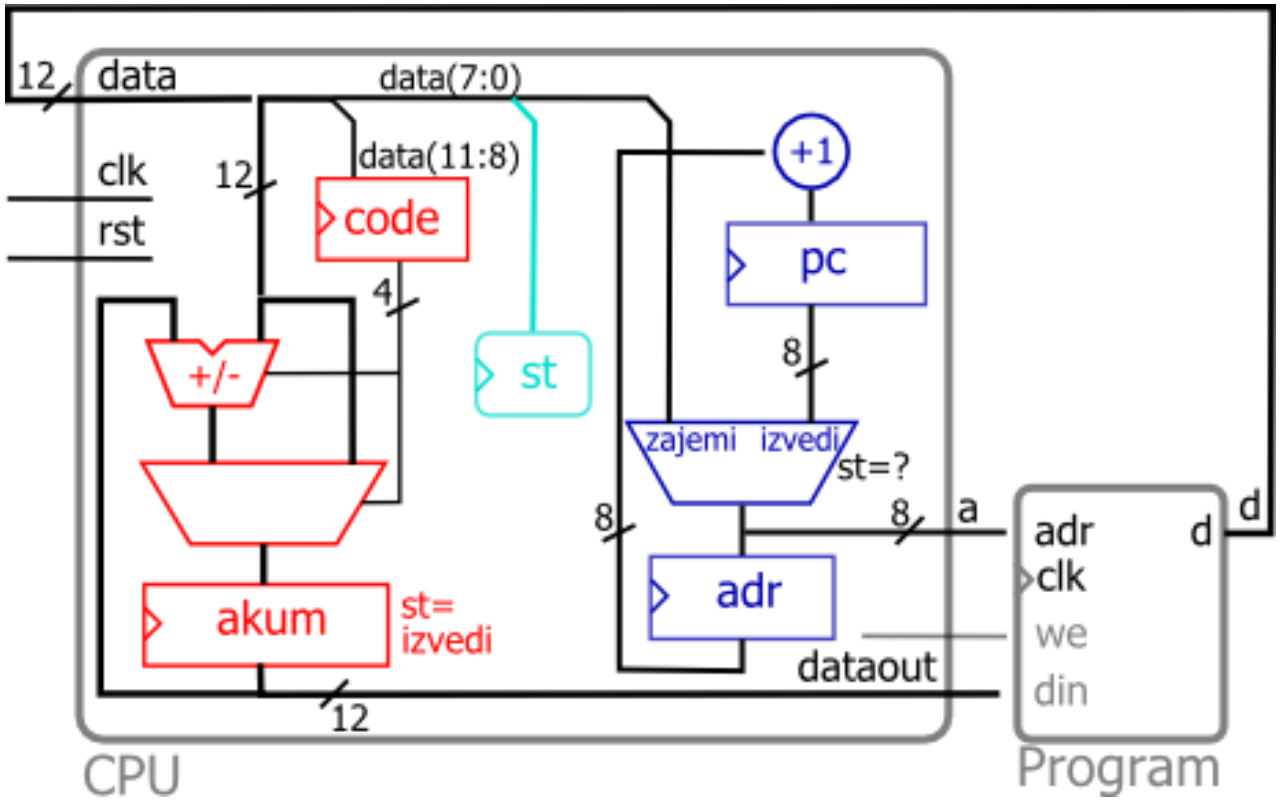
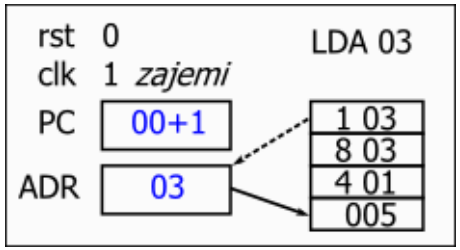

12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
adr
clk
we
din
d
d
akum
st=
izvedi
dataout
12
CPU
Program

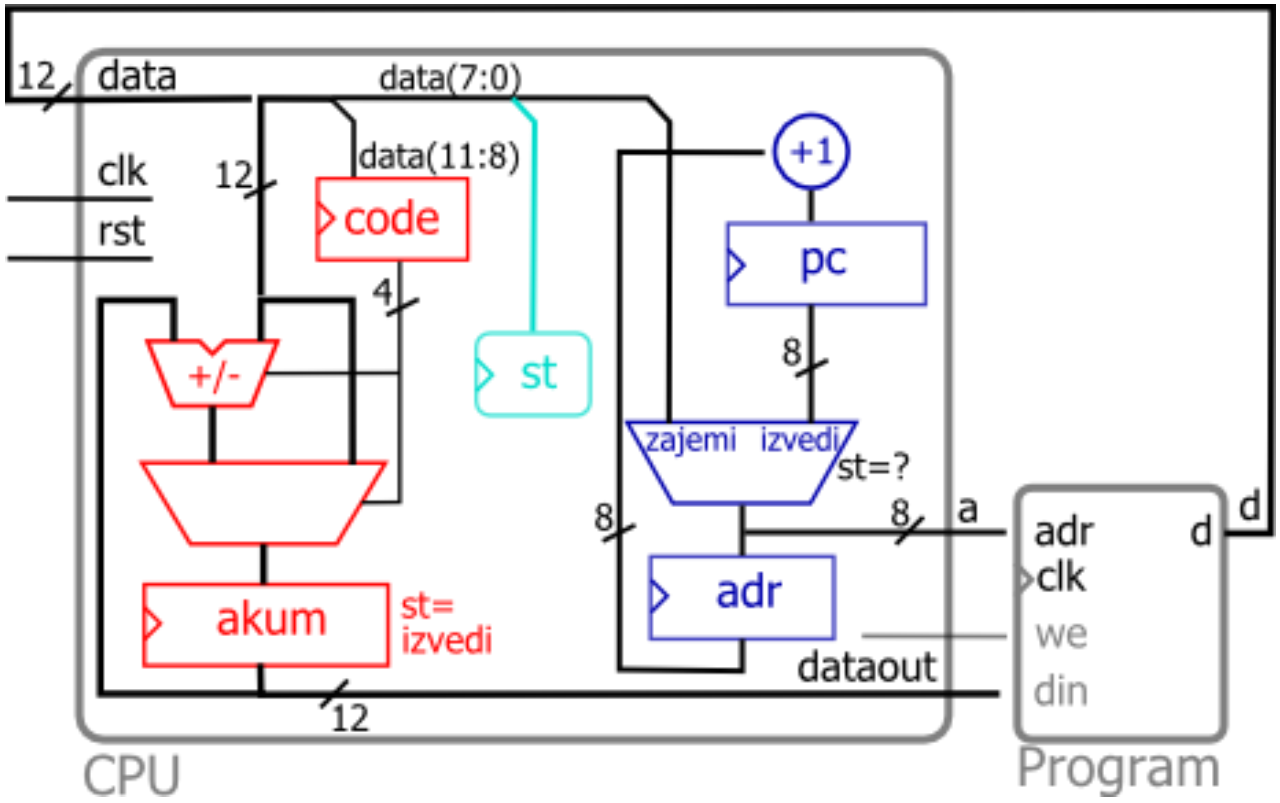

rst 1
clk 0 zajemi
PC
00
ADR
00
1 03
8 03
4 03
005

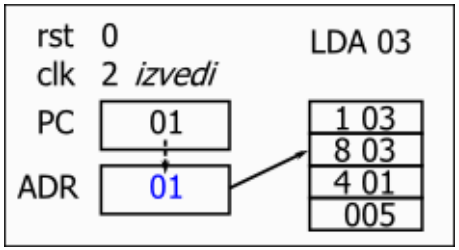
LDA 03


12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

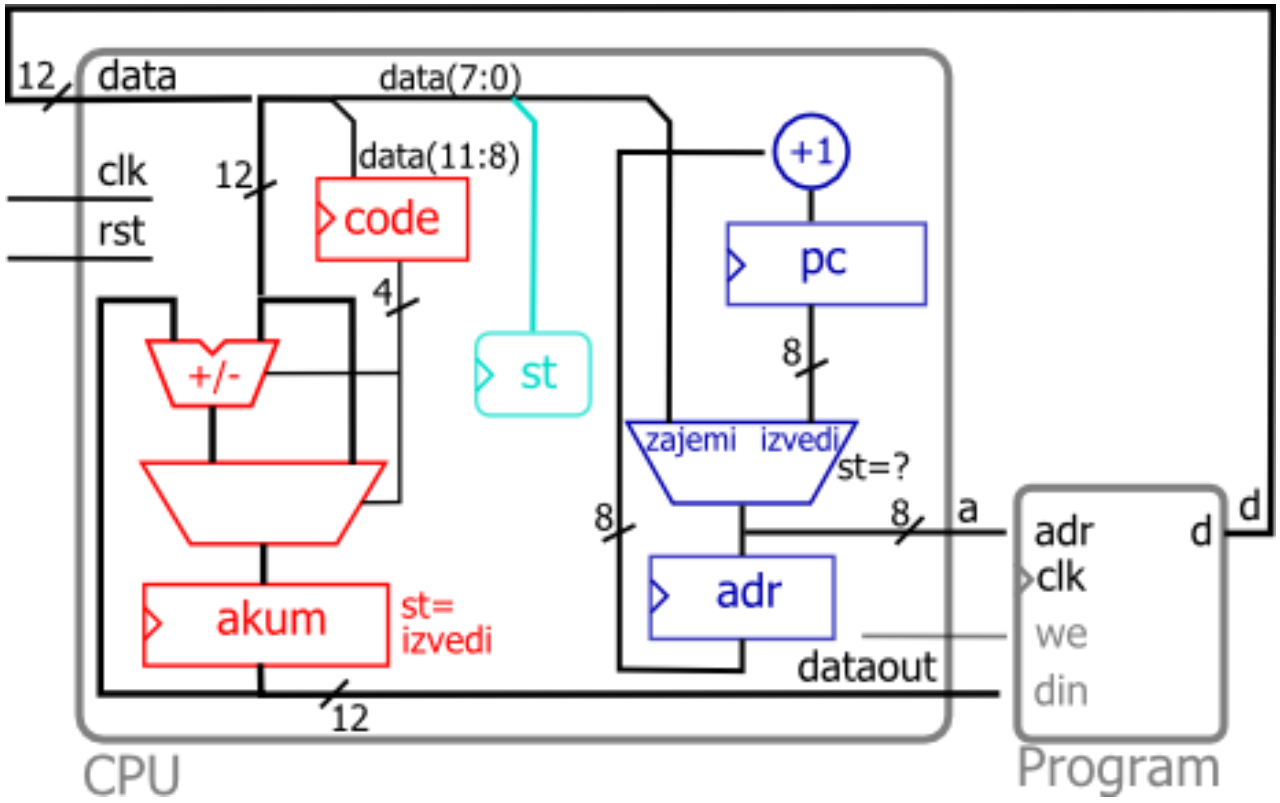

rst 0
clk 1 zajemi
LDA 03
PC
00+1
ADR
03
1 03
8 03
4 01
005

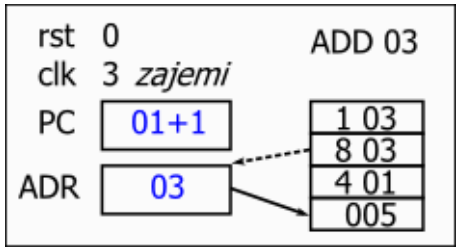
005

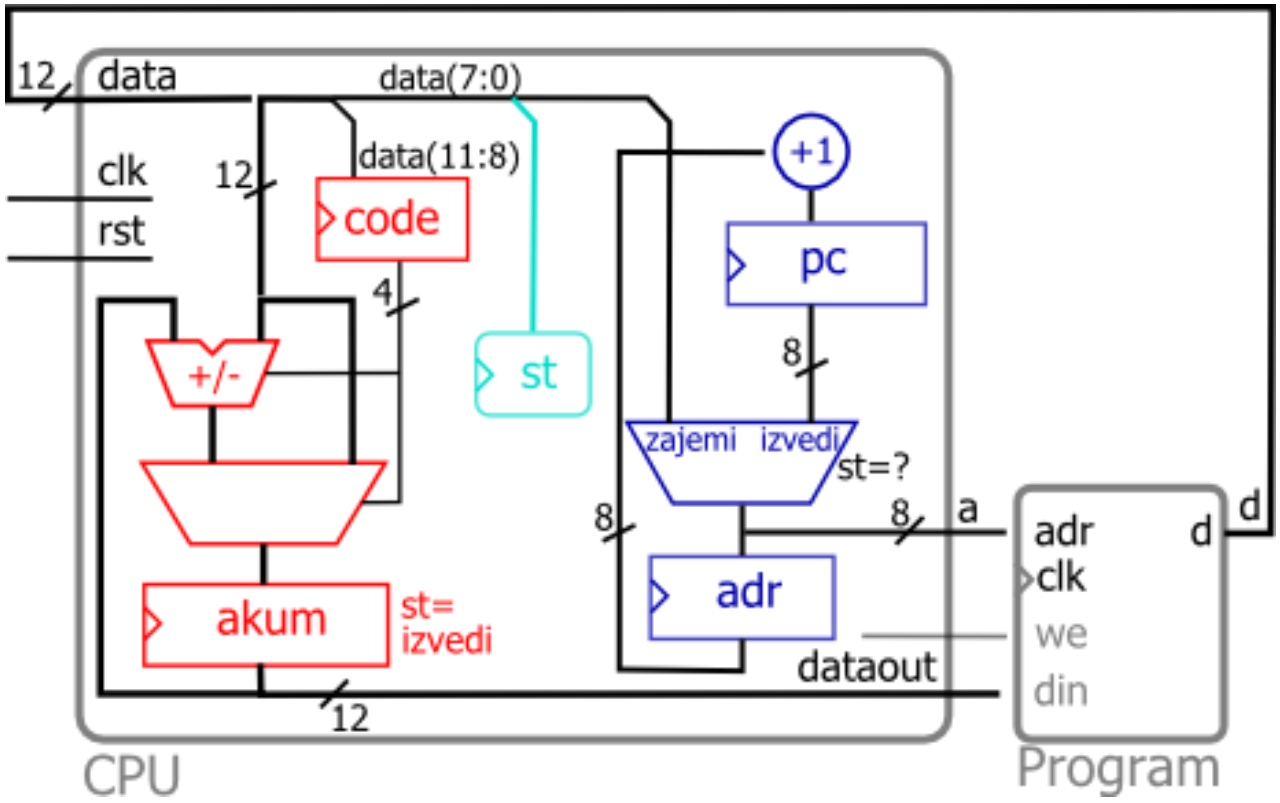

12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

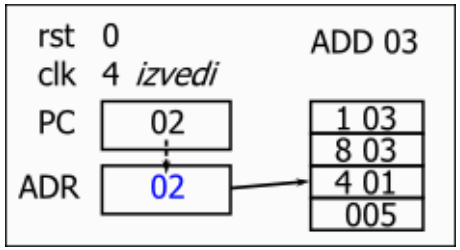

rst 0
clk 2 izvedi
LDA 03
PC
01
ADR
01
1 03
8 03
4 01
005

ADD 03

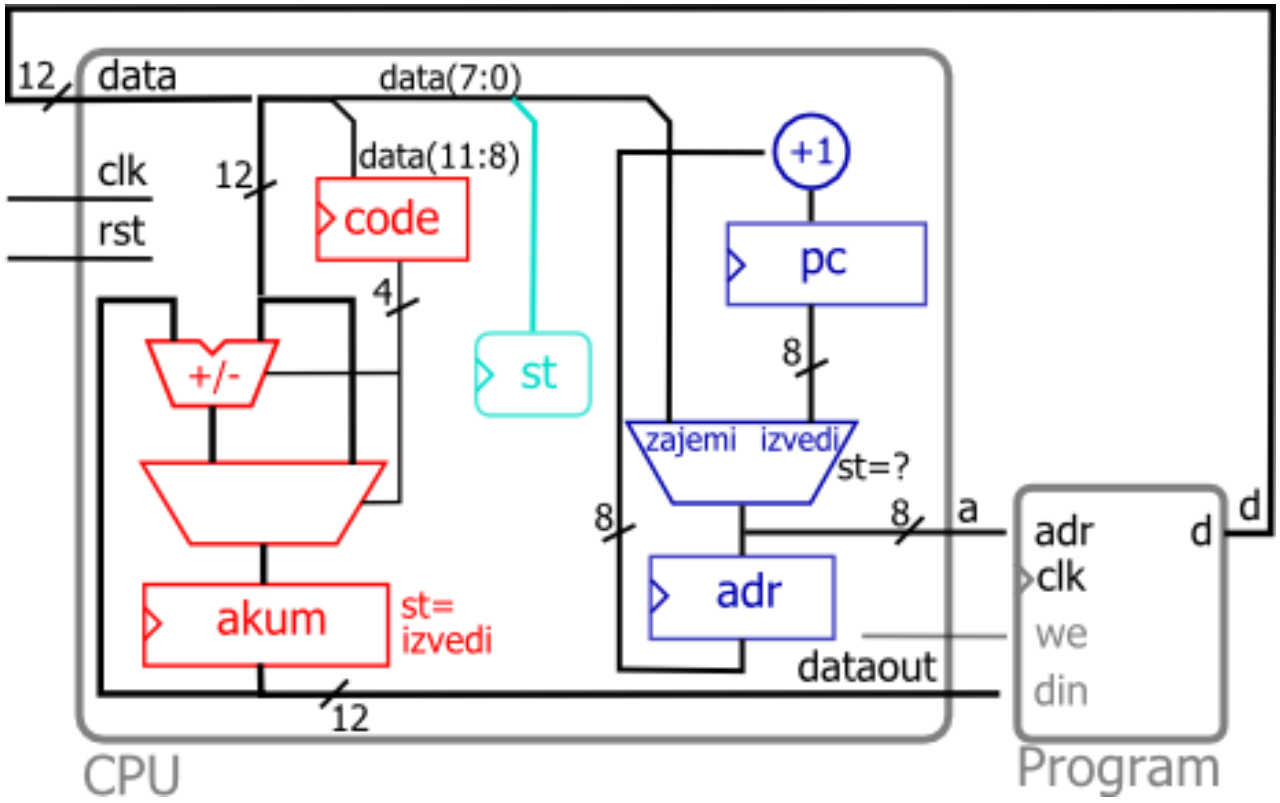

12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

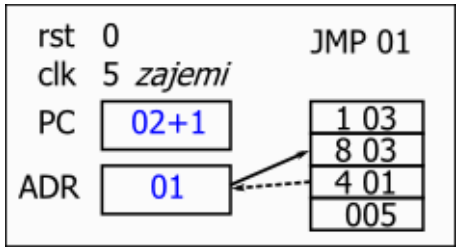

rst 0
clk 3 zajemi
ADD 03
PC
01+1
ADR
03
1 03
8 03
4 01
005


12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
adr
clk
we
din
d
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

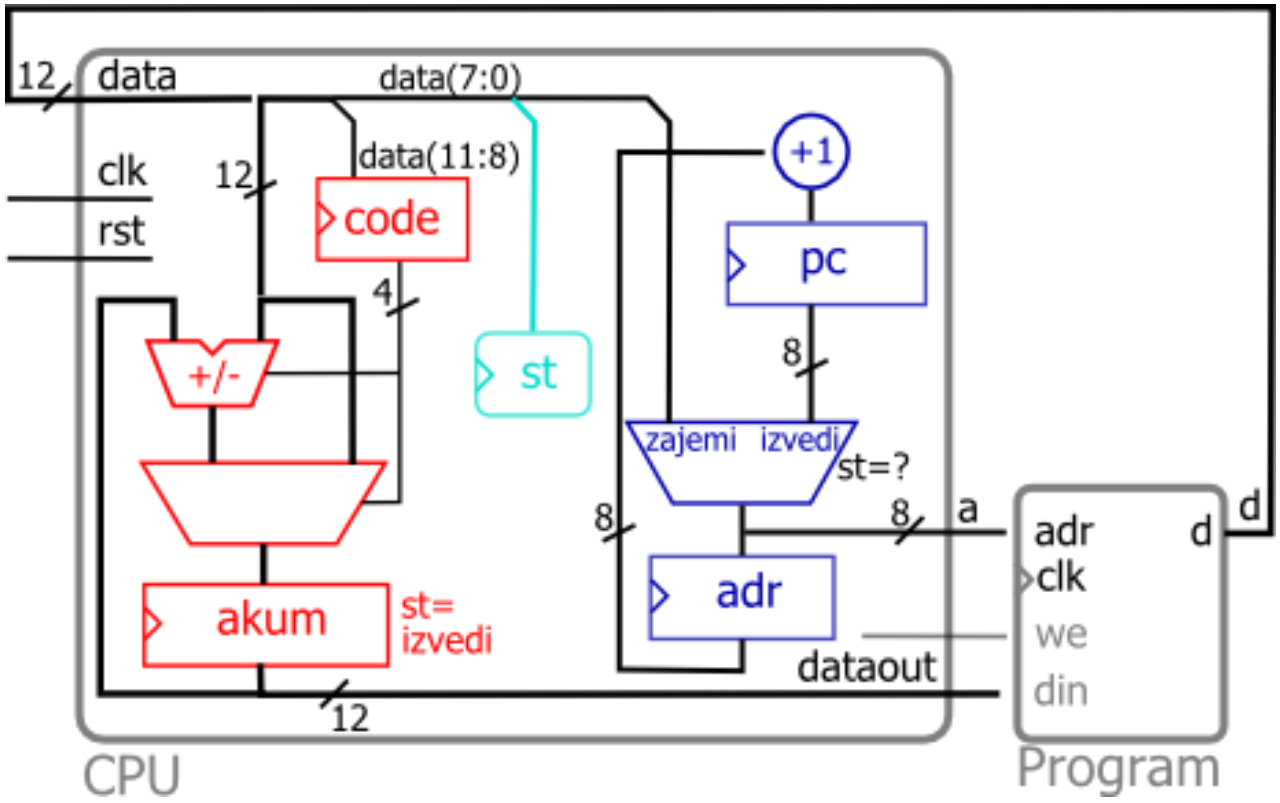

rst 0
clk 4 izvedi
ADD 03
PC
02
ADR
02
1 03
8 03
4 01
005

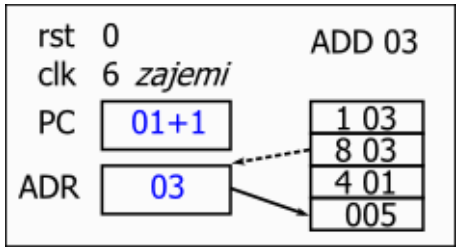
JMP 01


12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

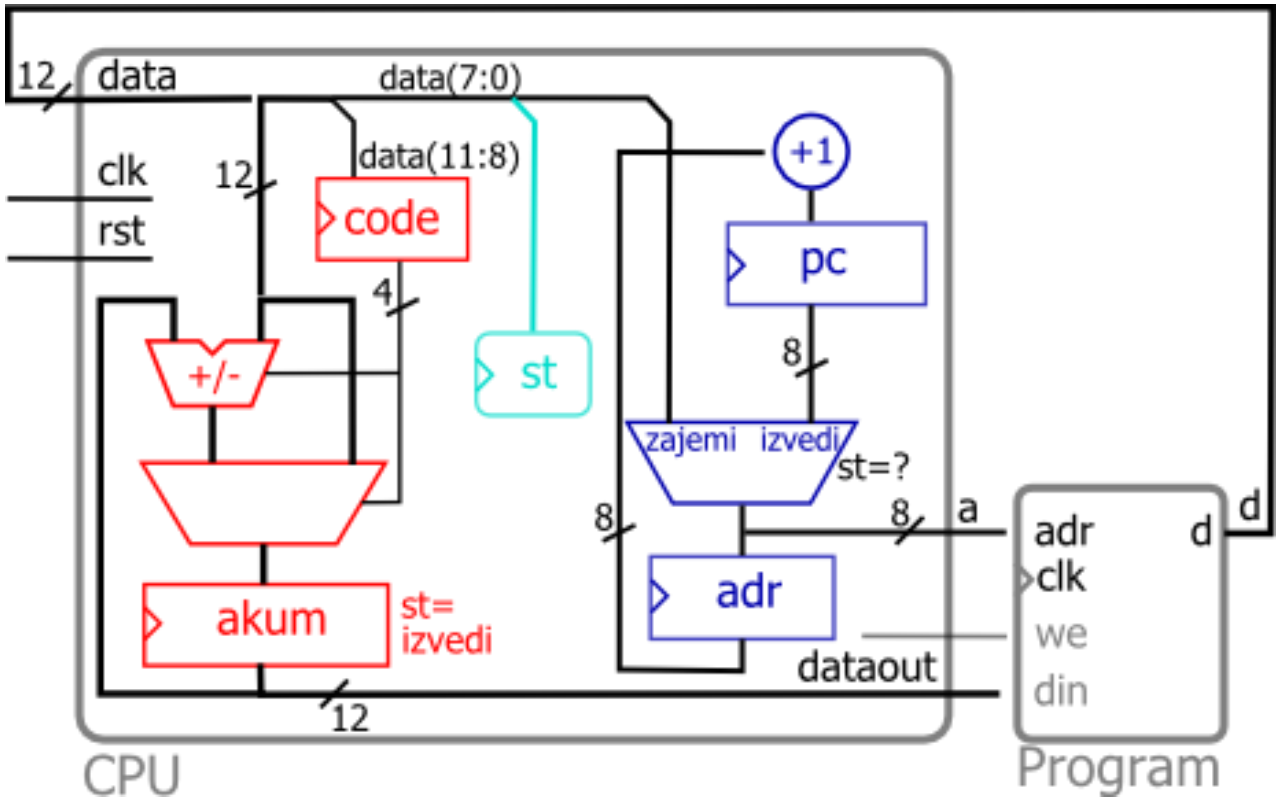

rst 0
clk 5 zajemi
JMP 01
PC
02+1
ADR
01
1 03
8 03
4 01
005

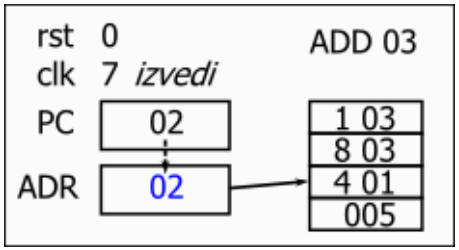
ADD 03


12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program

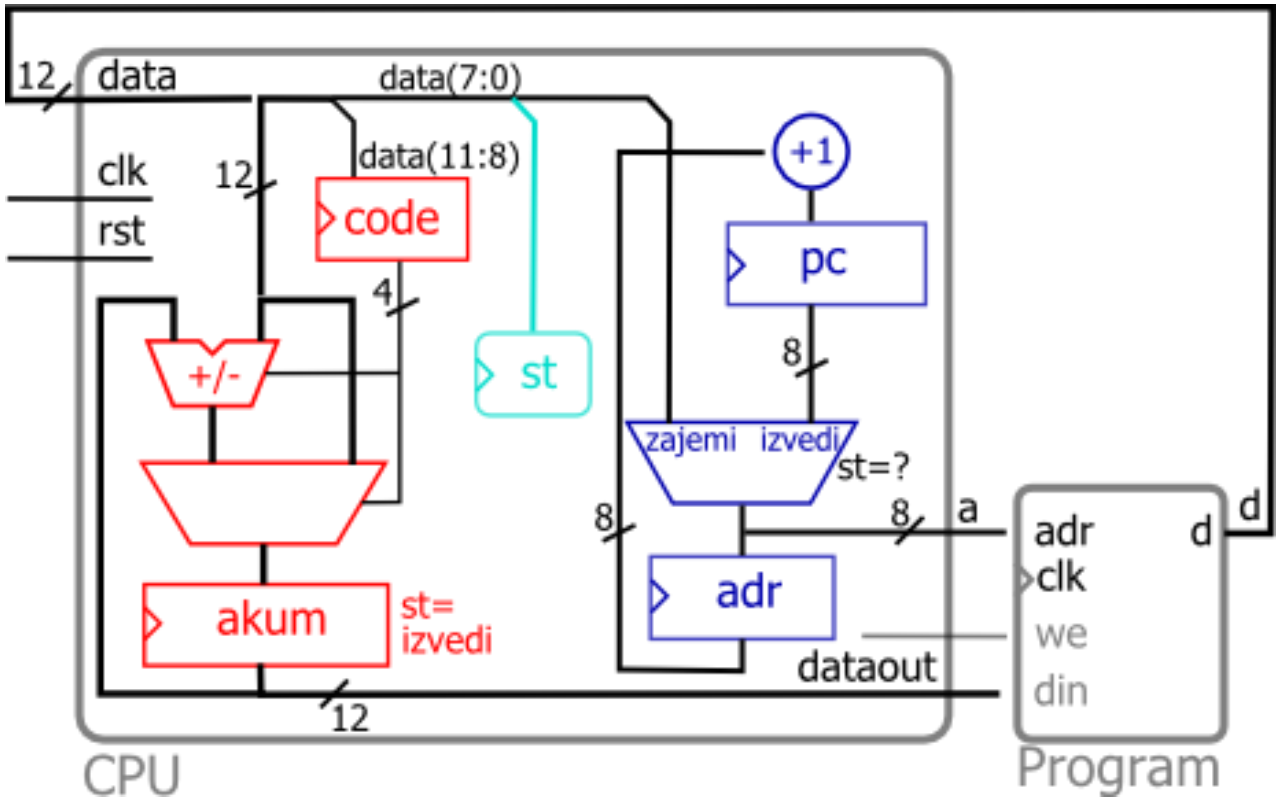

rst 0
clk 6 zajemi
ADD 03
PC
01+1
ADR
03
1 03
8 03
4 01
005

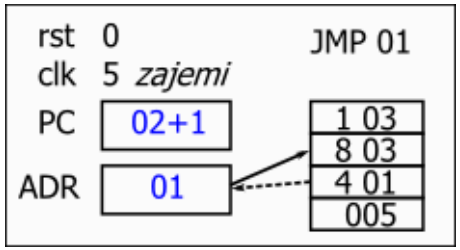
005

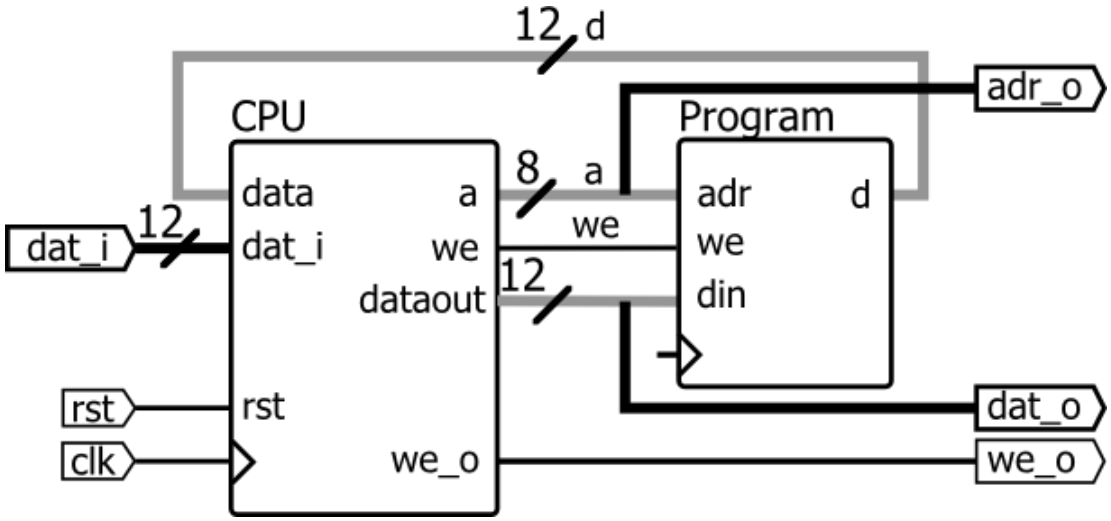

12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi
izvedi
st=?
8
8
a
adr
clk
we
din
d
d
akum
st=
izvedi
adr
dataout
12
CPU
Program


rst 0
clk 7 izvedi
ADD 03
PC
02
ADR
02
1 03
8 03
4 01
005

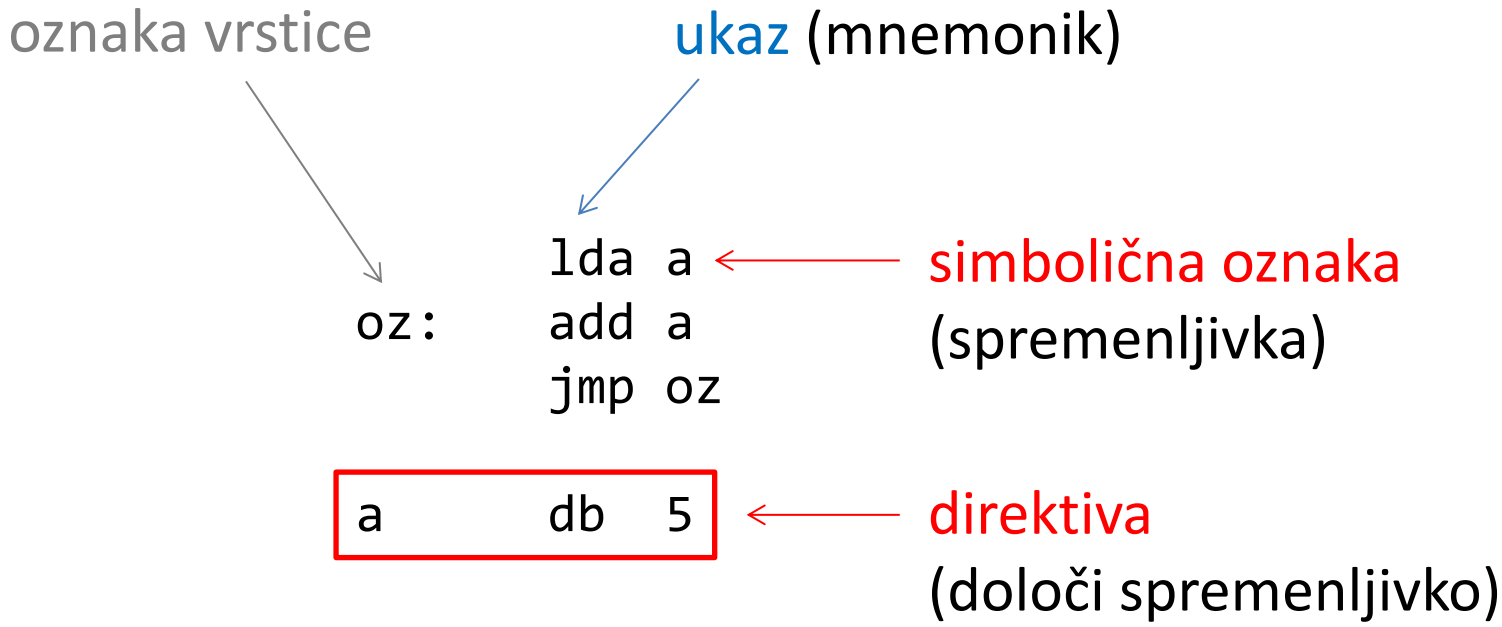
JMP 01


12
data
data(7:0)
clk
rst
12
data(11:8)
code
4
+/-
st
+1
pc
8
zajemi izvedi
st=?
8
8
a
d
adr
clk
we
din
d
akum
st=
izvedi
adr
dataout
12
CPU
Program


rst 0
clk 5 zajemi
JMP 01
PC
02+1
ADR
01
1 03
8 03
4 01
005


12
d
CPU
Program
adr_o
data
a
8
a
adr
d
12
dat_i
dat_i
we
we
din
12
dataout
rst
rst
dat_o
clk
we_o
we_o

Zbirnik in simulator CPU



Prevedena zbirniška koda:

```
0=> lda & x"03",
1=> add & x"03",
2=> jmp & x"01",
3=> x"005"
```