Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

Red Pitaya – elektronske orgle

DES 2017/18 - razvoj vgrajenega sistema

Elektronske orgle na vezju FPGA

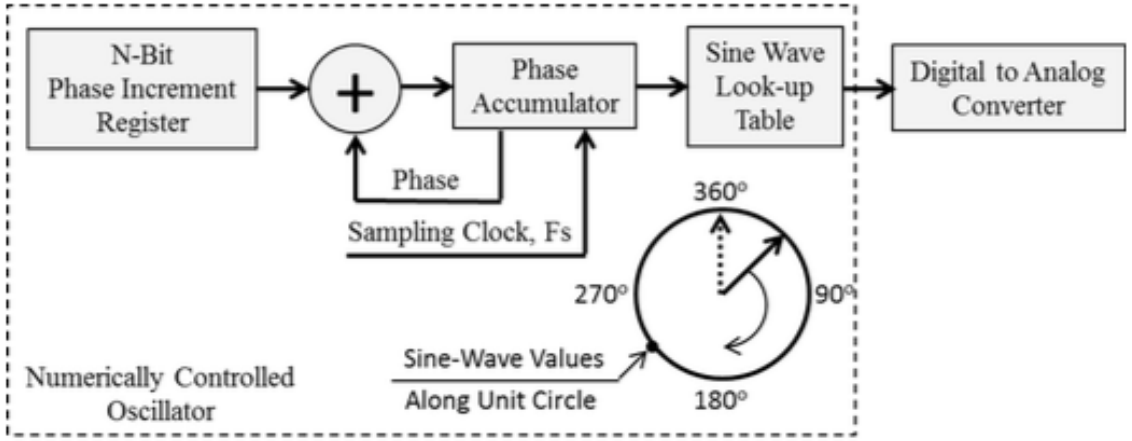
- načrtovanje generatorja tonov
- vmesnik za tipkovnico (PS/2)
- grafika za prikaz na zaslonu VGA

Altera DE0 Nano

Generator tonov v digitalnem vezju

1. Delilnik frekvence
   - naredimo števec po modulu M: števec šteje od 0 do M-1
   - izhodna frekvenca je določena s periodo obračanja števca, za izhod uporabimo najvišji bit ali pa doseg modula štetja

2. Numerično krmiljen oscilator
   - naredimo n-bitni števec, ki se povečuje za korak Δf
   - izhodna frekvenca je določena s periodo obračanja števca, uporabimo najvišji(e) bit(e) števca



https://occamtechgroup.com/2016/02/26/embedded-design-ideas-applying-direct-digital-synthesis-with-a-twist/

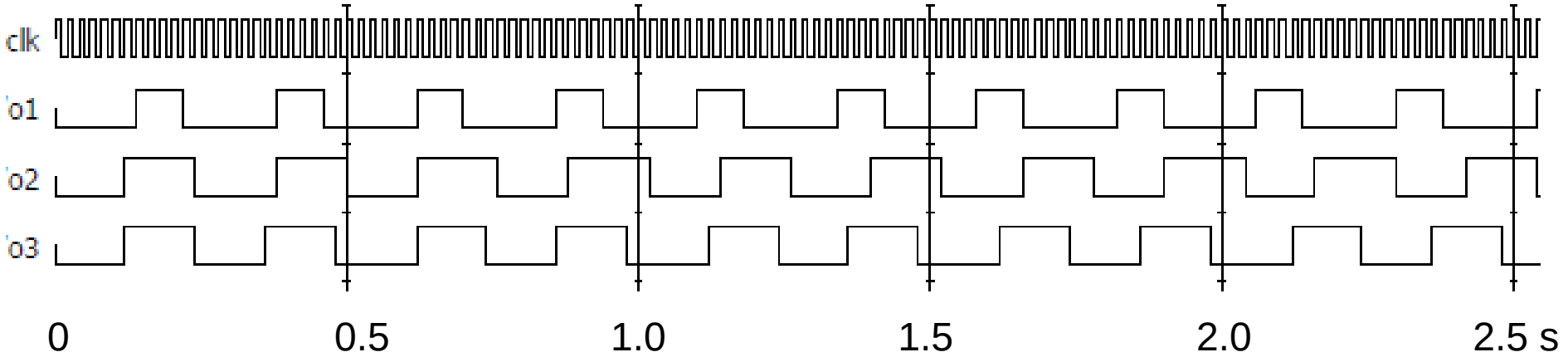
```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
USE ieee.math_real.all;

entity rom is
 port (
   adr : in unsigned(5 downto 0);
   data : out signed(7 downto 0)
 );
end rom;

architecture Behavioral of rom is
 constant romsize: integer := 64; -- stevilo elementov sinusne tabele

 type sintab is array(0 to romsize-1) of signed(7 downto 0);
 signal sinrom: sintab;
begin

 -- generator vsebine sinusne tabele
 g: for i in 0 to romsize-1 generate
 constant sinval: signed (7 downto 0) :=
to_signed(integer(127.0*sin(real(i)*2.0*math_pi/real(romsize))),8);
 begin
  sinrom(i) <= sinval;
 end generate;

 -- tabela kot pomnilnik ROM
 data <= sinrom(to_integer(adr));

end Behavioral;
```

Primerjava delilnika in numeričnega oscilatorja

Vhod: 50 Hz, izhod: 4 Hz (razmerje 12.5)

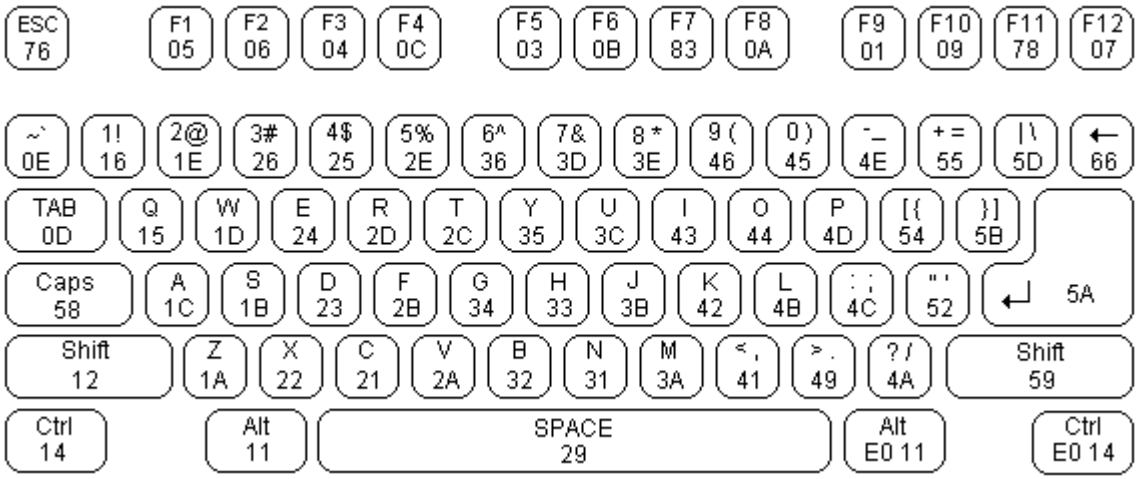
- delilnik: 12 => 4.16 Hz ali 13 => 3.84 Hz
- NCO: 6-bit, Δf=5 => 3.906 Hz

  10-bit, Δf=82 => 4.004 Hz



Vmesnik PS/2

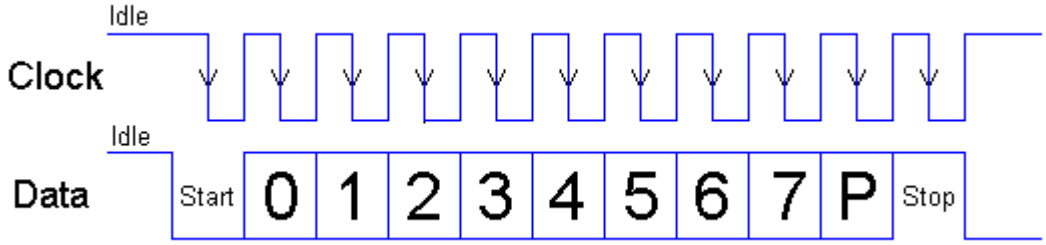
- Zaporedni vmesnik za branje tipkovnice
  - tipkam so dodeljene scan kode



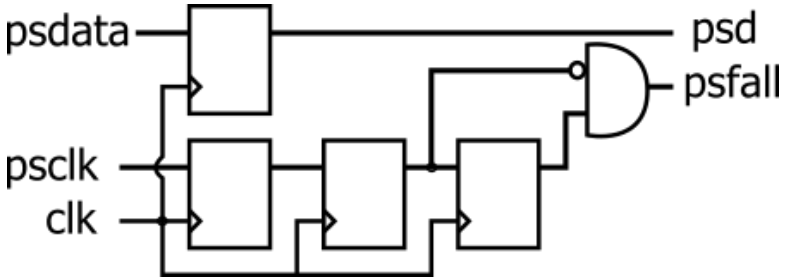
PS/2

1. KBD Clock
2. GND
3. KBD Data
4. N/C
5. +5V (VCC)
6. N/C

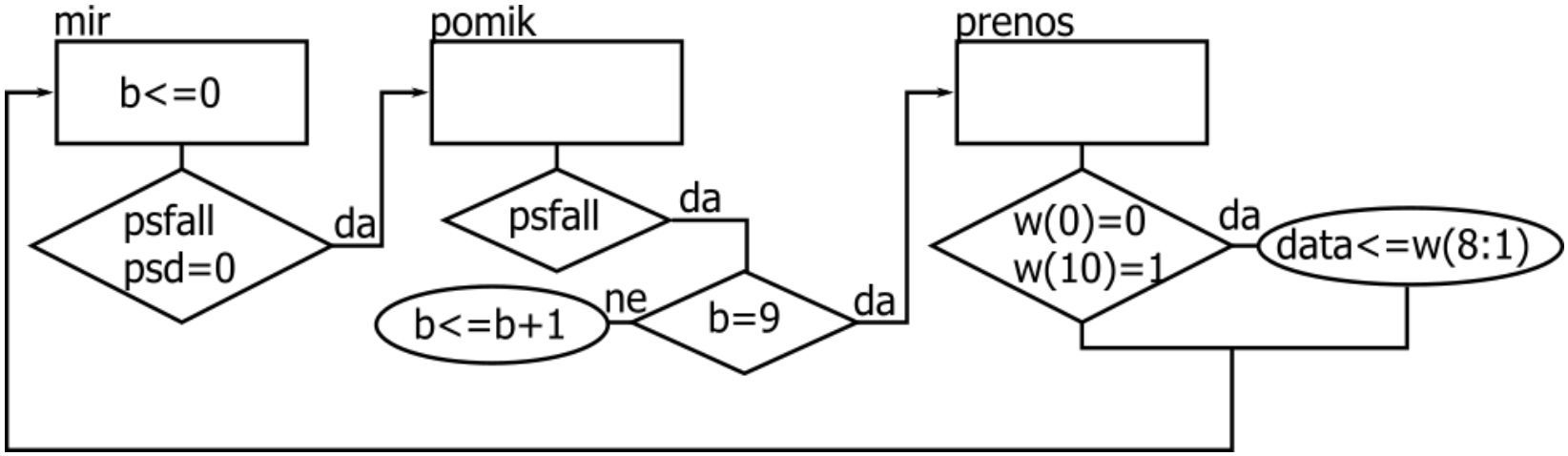
- zaporedje: start ('0'), podatkovni biti od LSB do MSB, liha pariteta in stop ('1')



Sinhrono zaznavanje PS/2 prehodov



- Algoritmični sekvenčni stroj za sprejem podatkov



```
stim_proc: process
  procedure oddaj (D : std_logic_vector(7 downto 0)) is
  begin
    psdata <= '0'; -- Start bit
    wait for (PS2Period / 2);
    psclk  <= '0'; wait for (PS2Period / 2);
    psclk  <= '1';

    for i in 0 to 7 loop -- Data Bits
      psdata <= D(i);
      wait for (PS2Period / 2);
      psclk  <= '0'; wait for (PS2Period / 2);
      psclk  <= '1';
    end loop;

    psdata <= odd(D); -- Odd Parity bit
    wait for (PS2Period / 2);
    psclk  <= '0'; wait for (PS2Period / 2);
    psclk  <= '1';

    psdata <= '1'; -- Stop bit
    wait for (PS2Period / 2);
    psclk  <= '0'; wait for (PS2Period / 2);
    psclk  <= '1';
    wait for (PS2Period * 3);
  end procedure oddaj;

begin
 psdata <= '1';
 psclk  <= '1';
 wait for (PS2Period * 3);

 oddaj(x"F0");
```

Primer opisa komponente IP: I2C vmesnik

Opis namena in lastnosti komponente

The I^2C is a two-wire, bi-directional serial bus, which provides simple and efficient method of data transmission over short distance, between many devices. The DI2CM core provides an interface between a microprocessor / microcontroller and an I^2C bus. It can work as a master transmitter or a master receiver - depending on a working mode determined by the microprocessor / microcontroller.

KEY FEATURES

- Conforms to v.4.0 of the I^2C specification
- Master operation
  - *Master transmitter*
  - *Master receiver*
- Support for all transmission speeds
  - *Standard (up to 100 kb/s)*
  - *Fast (up to 400 kb/s)*

DELIVERABLES

- Source code:
  - VHDL Source Code
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment

Blokovna shema in opis gradnikov

Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.

Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.

Control Register – Contains five control bits, used for performing all types of I^2C Bus transmissions.

Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CM core.

Clock Generator – Performs generation of the serial clock.

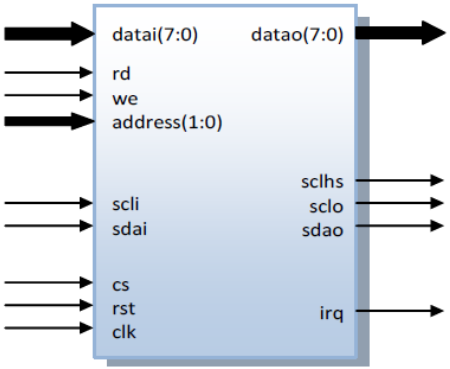
Input Filter – Performs spike filtering.

Clock Synchronization – Performs clock synchronization.

Arbitration Logic – Performs arbitration during operations in multi-master systems.

Timer – Allows operation from a wide range of the input frequencies. It is programmed by the user before transmission and can be reprogrammed to change the SCL frequency.

Shema in opis priključkov



Rezultati sinteze (lastnosti vezja v izbrani tehnologiji)

Family	Device	Speed grade	LUT	Slice	F_{max}
SPARTAN-3	xc3s50	-5	271	194	161 MHz
SPARTAN-3E	xc3s100e	-5	264	190	162 MHz
SPARTAN-6	xc6slx4	-3	173	75	270 MHz

https://dcd.pl/workspace/documentation/xil/di2cm_ds.pdf