

Laboratorij za načrtovanje integriranih vezij

Univerza v Ljubljani
Fakulteta *za elektrotehniko*



Andrej Trost

Uvod v laboratorijske vaje 2020/21

Integrirana vezja Načrtovanje digitalnih elektronskih sistemov

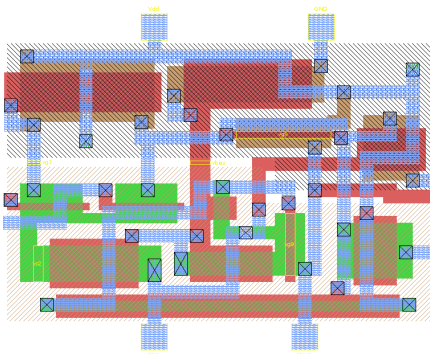
<https://lniv.fe.uni-lj.si/b.html>

<https://lniv.fe.uni-lj.si/altera/>

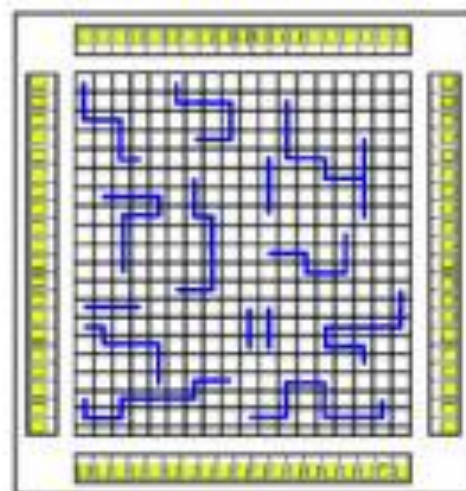
Digitalna integrirana vezja - tehnologija

- ▶ razvoj popolnoma naročniških digitalnih integriranih vezij je zelo zahteven
- ▶ nekatere tehnološke izvedbe omogočajo avtomatizacijo:
 - ▶ uporaba standardnih celic ali polja vrat
 - ▶ Electronic Design Automation tools

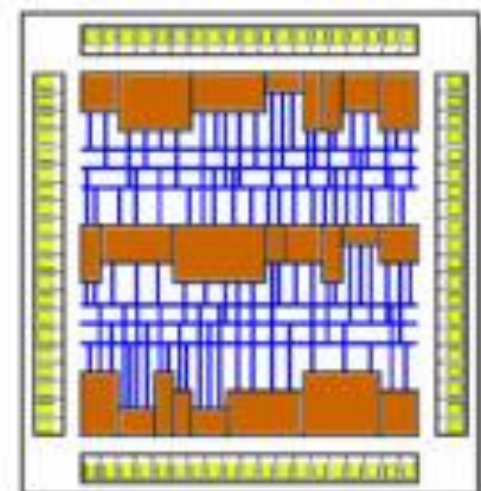
naročniška



polje vrat



standardne celice

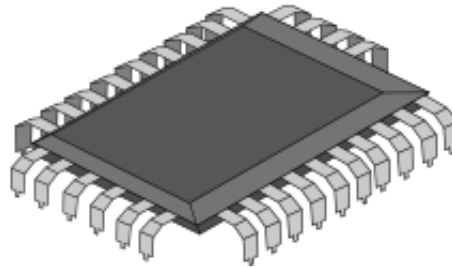


Digitalna integrirana vezja - funkcija

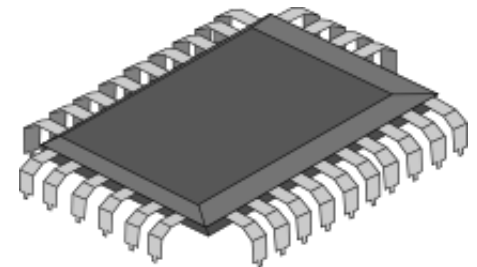
logični gradniki 74nn



mikroprocesor



namensko vezje
ASIC

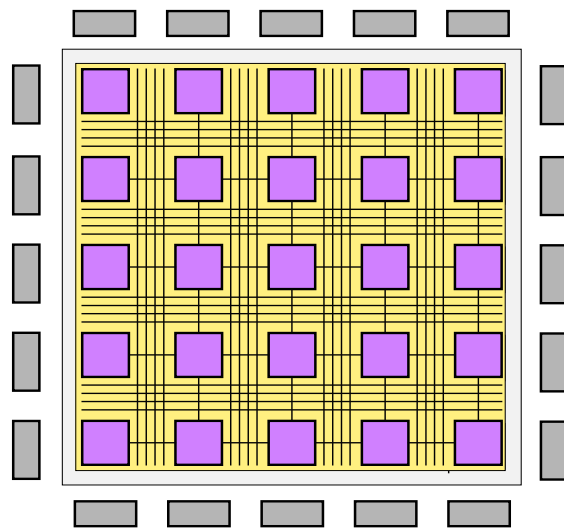


Po funkciji jih delimo na:

- ▶ enostavne logične gradnike
- ▶ vezja za specifičen namen (Application Specific IC)
- ▶ univerzalna vezja, npr. mikroprocesorji

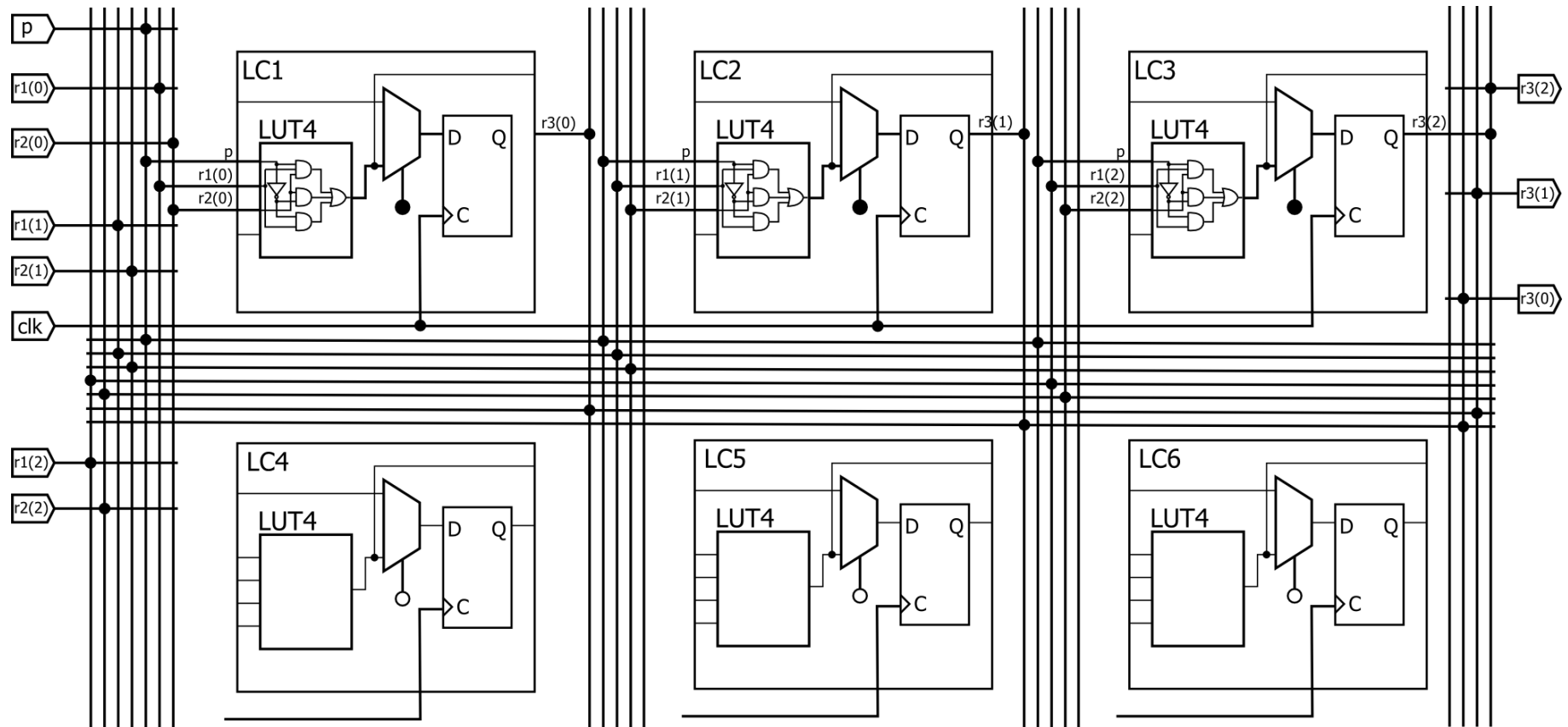
Programirljiva vezja **FPGA**

- ▶ programirljiva vezja omogočajo razvoj namenskega vezja z vnaprej izdelanim čipom
- ▶ hiter razvoj, univerzalnost, hitra obdelava signalov in odziv
- ▶ paralelno delovanje
- ▶ standarden opis vezja (VHDL, Verilog)

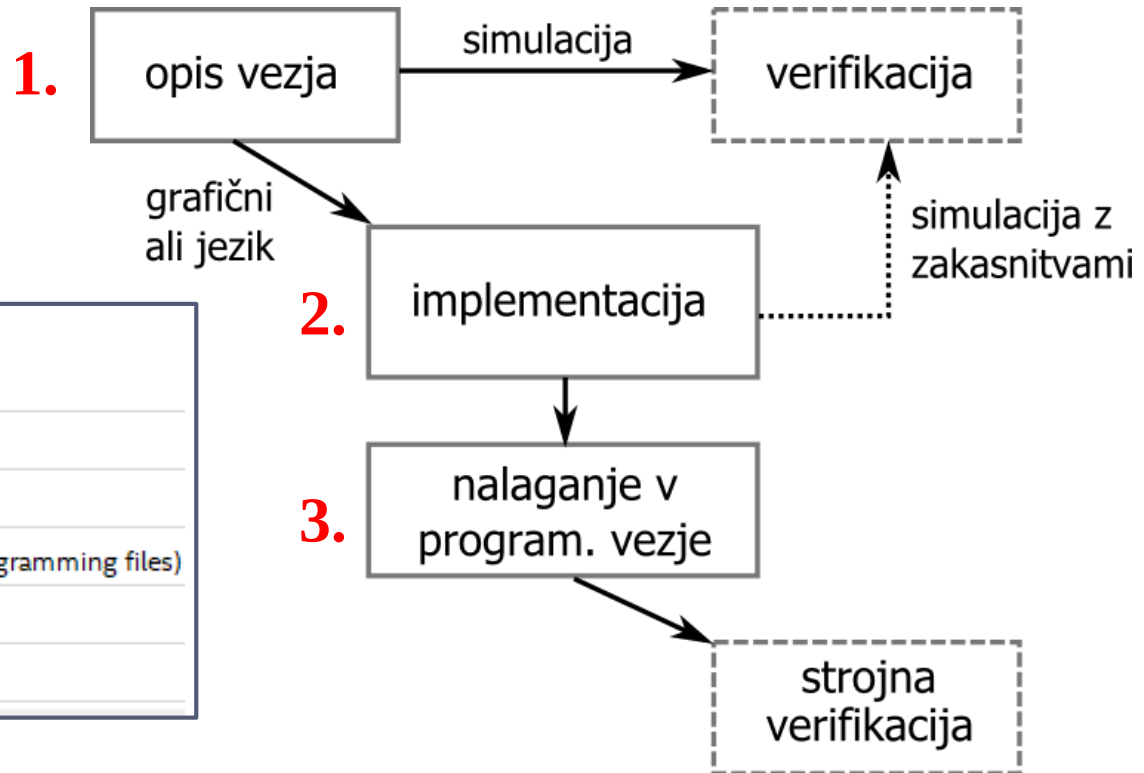


Field Programmable Gate Array

- ▶ določimo vsebino in povezave v logičnih celicah
- ▶ vzpostavimo povezave v matriki in z zunanjimi priključki
- ▶ **postopek tehnološke preslikave je avtomatiziran!**



Koraki dela z orodji za vezja FPGA



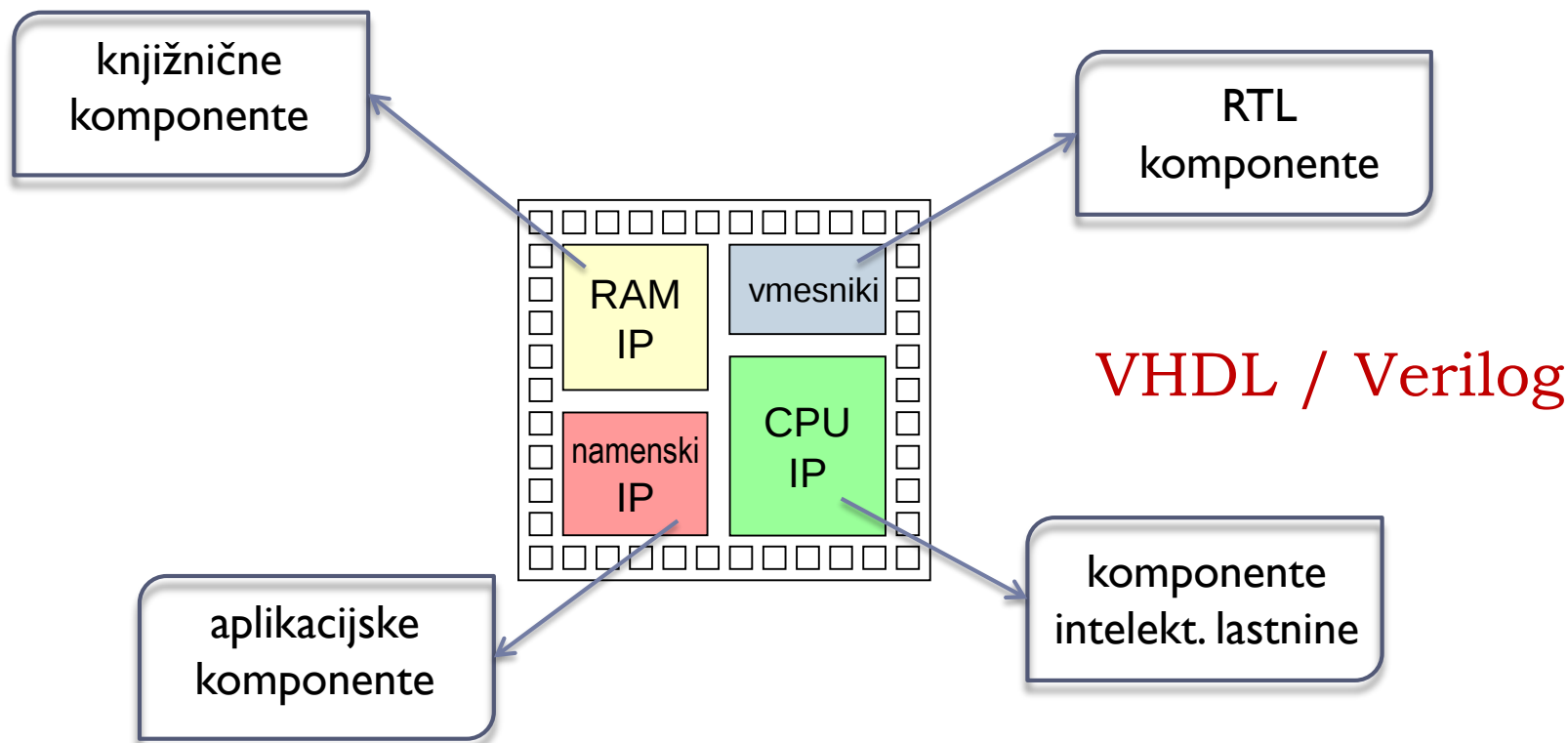
	Task
	▼ ► Compile Design
✓	> ► Analysis & Synthesis
	> ► Fitter (Place & Route)
	> ► Assembler (Generate programming files)
	> ► Timing Analysis
	> ► EDA Netlist Writer



Altera DE0 Nano

Razvoj digitalnega vezja / sistema

- ▶ sistemi iz vnaprej pripravljenih komponent (knjižnica, IP) in specifičnih vezij
- ▶ vezja z natančnimi časovnimi parametri in omejitvami sintetiziramo iz opisa VHDL ali Verilog



Študent bo znal:

Opisati logično vezje

- ▶ strukturno (shema)
- ▶ funkcijsko
- ▶ RTL in
- ▶ postopkovno
- ▶ razviti preprost CPU, ki izvaja algoritem v strojni kodi
- ▶ uporabljati orodja za FPGA
- ▶ izdelati sistem z vmesniki in namensko logiko v VHDL

Tema: funkcijski generator

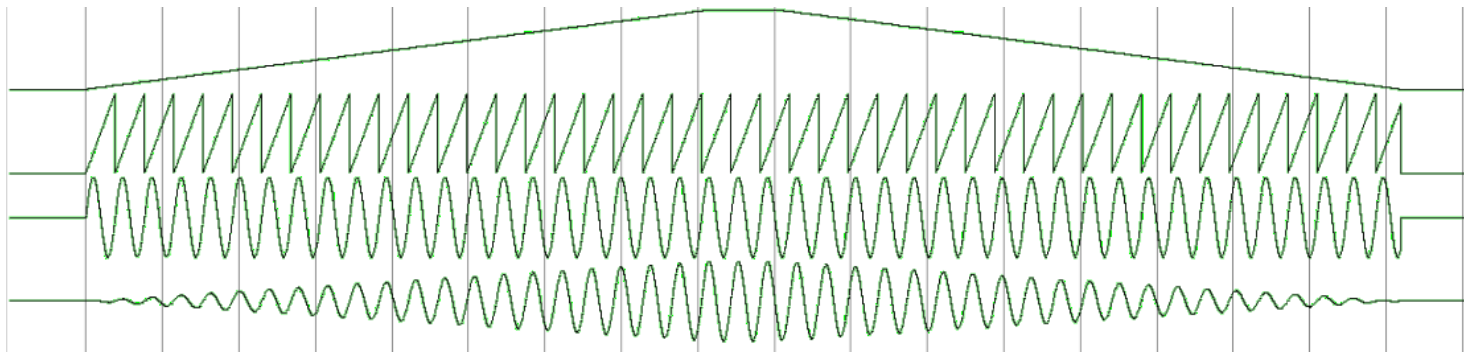
- ▶ modeli osnovnih vezij
- ▶ sekvenčni stroj

Projekt IV:

- ▶ 12-bitni mikroprocesor
- ▶ periferne enote
- ▶ digitalni sintetizator

Projekt NDES:

- ▶ funkcijski generator



Imenovanje programske opreme

<https://www.altera.com/products/design-software/fpga-design/quartus-prime/download.html>

The screenshot shows the Intel Quartus Prime Software download page. The page has a blue header with the Intel logo and navigation links. Below the header, there's a section titled 'Download Intel® Quartus® Prime Software' with a sub-header 'Three Intel® Quartus® Prime Editions to Meet Your System Design Requirements'. The page is divided into three columns, each representing a different edition of the software:

- Pro Edition:** The Intel® Quartus® Prime Pro Edition Software supports the advanced features in Intel's next-generation FPGAs and SoCs with the Intel® Agilex™, Intel® Stratix® 10, Intel® Arria® 10, and Intel® Cyclone® 10 GX device families. A blue button labeled 'Download now (paid license required) →' is at the bottom.
- Standard Edition:** The Intel® Quartus® Prime Standard Edition software includes extensive support for earlier device families in addition to the Intel® Cyclone® 10 LP device family. A blue button labeled 'Download now (paid license required) →' is at the bottom.
- Lite Edition:** The Intel® Quartus® Prime Lite Edition software supports Intel's low-cost FPGA device families. A blue button labeled 'Download now (free, no license required) →' is at the bottom, with a red arrow pointing to it.

- ▶ potrebna je brezplačna registracija na spletni strani

Select edition: Lite
Select release: 20.1



► nastavitve za prenos programske opreme

Operating System Windows Linux

- ✓ The Quartus Prime Lite Edition Design Software, Version 20.1 includes functional and security updates. Users should keep their software up-to-date and follow the [technical recommendations](#) to help improve security. Additional security updates are planned and will be provided as they become available. Users should promptly install the latest version upon release.
- ✓ The Quartus Prime Lite Edition Design Software, Version 20.1 is subject to removal from the web when support for all devices in this release are available in a newer version, or all devices supported by this version are obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [subscribe to our customer notification mailing list](#).
- ✓ The Quartus Prime Lite Edition Design Software, Version 20.1 supports the following device families: Arria II, Cyclone 10 LP, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. [▼ More](#)

Combined Files Individual Files Additional Software

Download and install instructions: [▼ More](#)
[Read Intel FPGA Software v20.1 Installation FAQ](#)
[Quick Start Guide](#)

Quartus Prime Lite Edition (Free)
Quartus Prime (includes Nios II EDS)
Size: 1.6 GB MD5: 23479E4E46326A05C4EC63D0E6B6F192
** Nios II EDS on Windows requires Ubuntu 18.04 LTS on Windows Subsystem for Linux (WSL), which requires a manual installation.
** Nios II EDS requires you to install an Eclipse IDE manually.
ModelSim-Intel FPGA Edition (includes Starter Edition)
Size: 1.2 GB MD5: D5E635E3229104088B0185D920ACC694

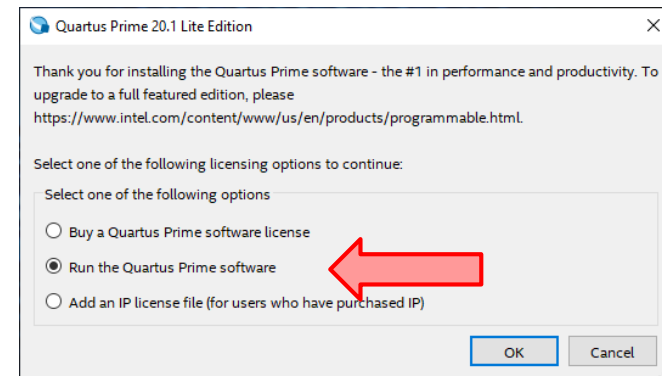
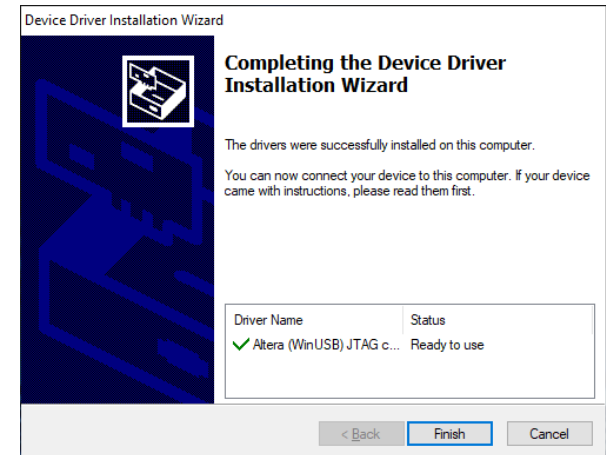
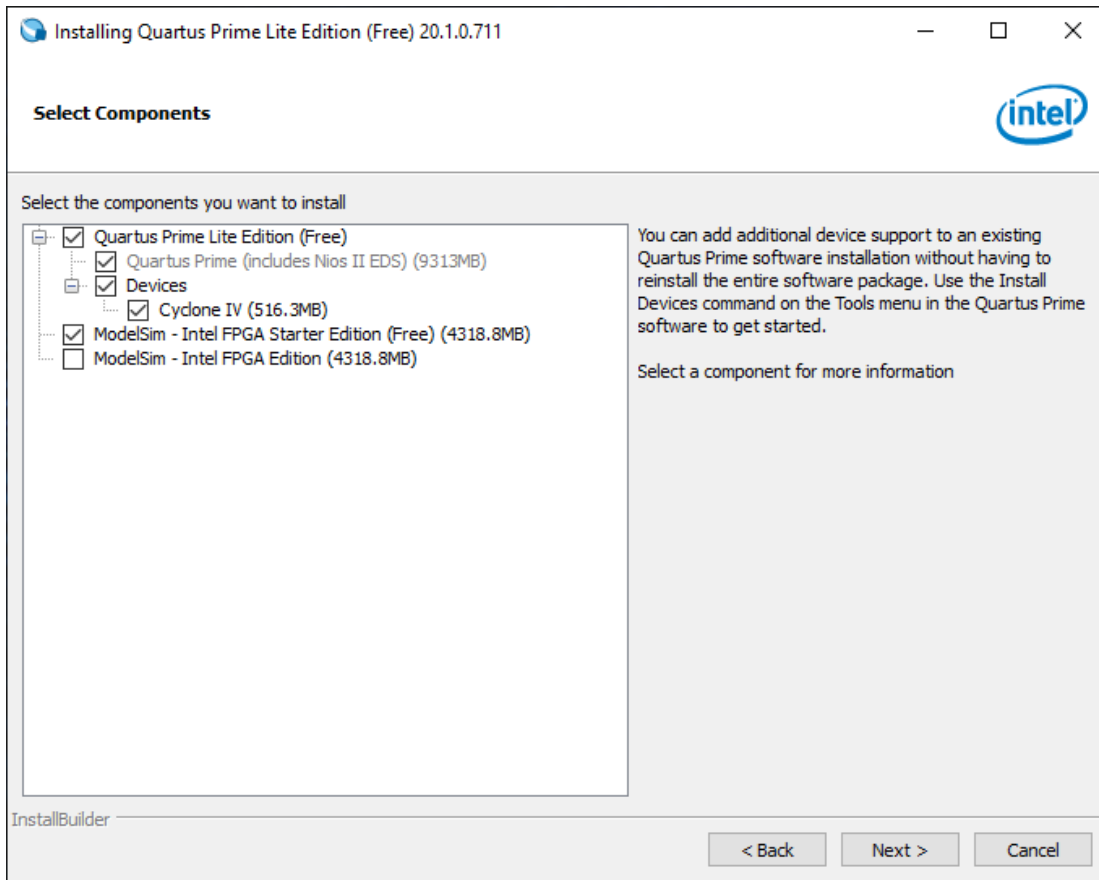
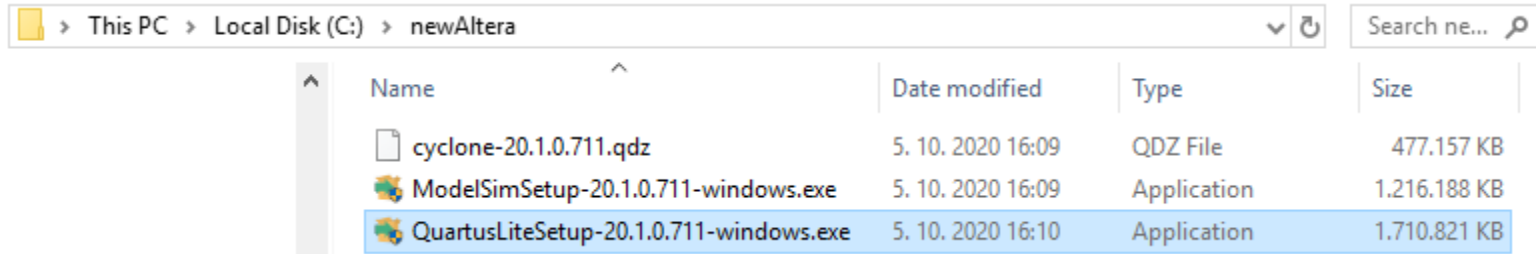
Devices
You must install device support for at least one device family to use the Quartus Prime software.
Arria II device support
Size: 499.1 MB MD5: A439BB4873E69BD23E35ACED3EA9BA8C
Cyclone IV device support
Size: 466.0 MB MD5: 14E47510CEA47DC0ED92C8CB97D76488



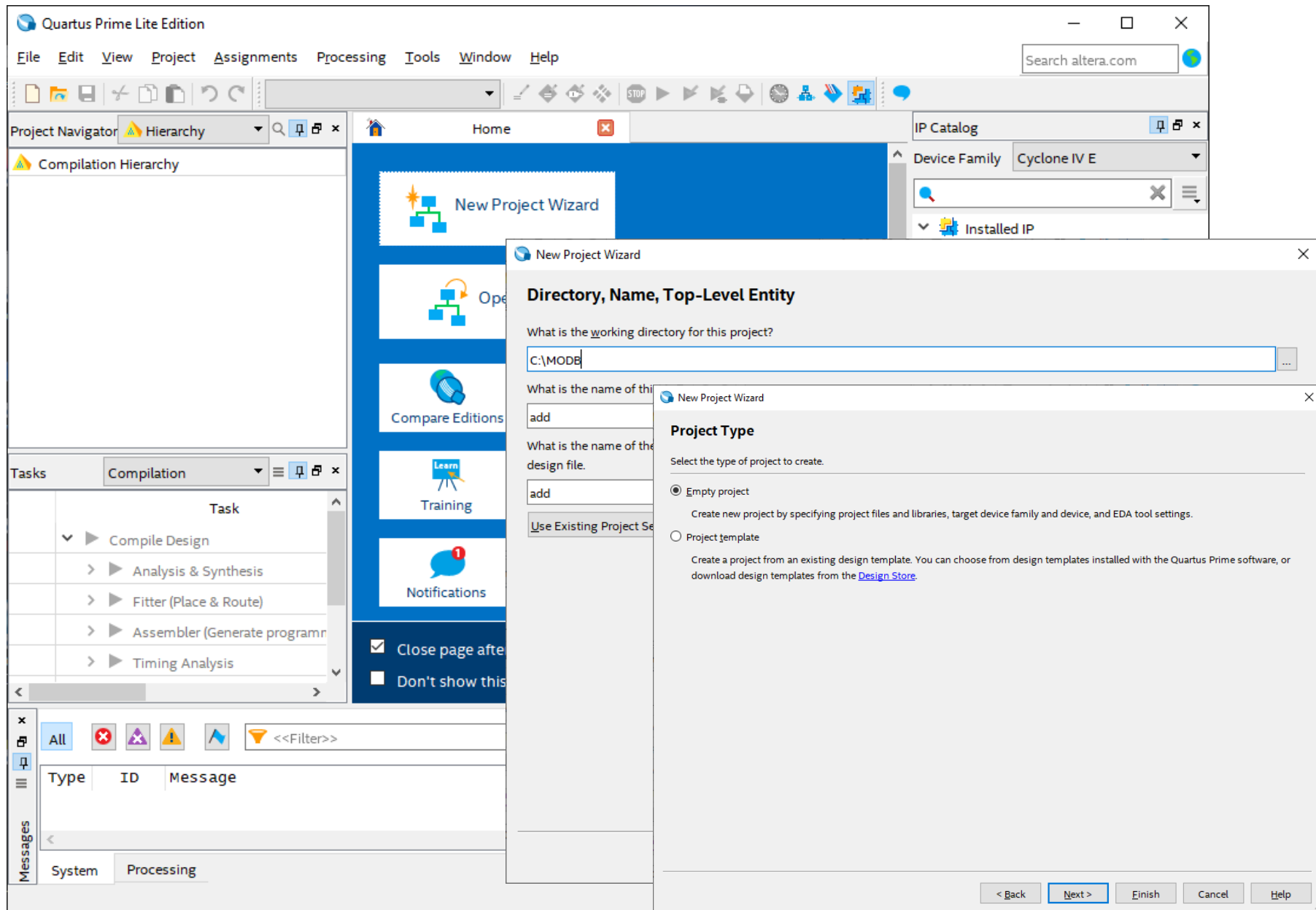
Note: The Quartus Prime software is a full-featured EDA product. Depending on your download speed, download times may be lengthy.

Namestitev Quartus Prime Lite

Program zasede 14 GB prostora na disku !

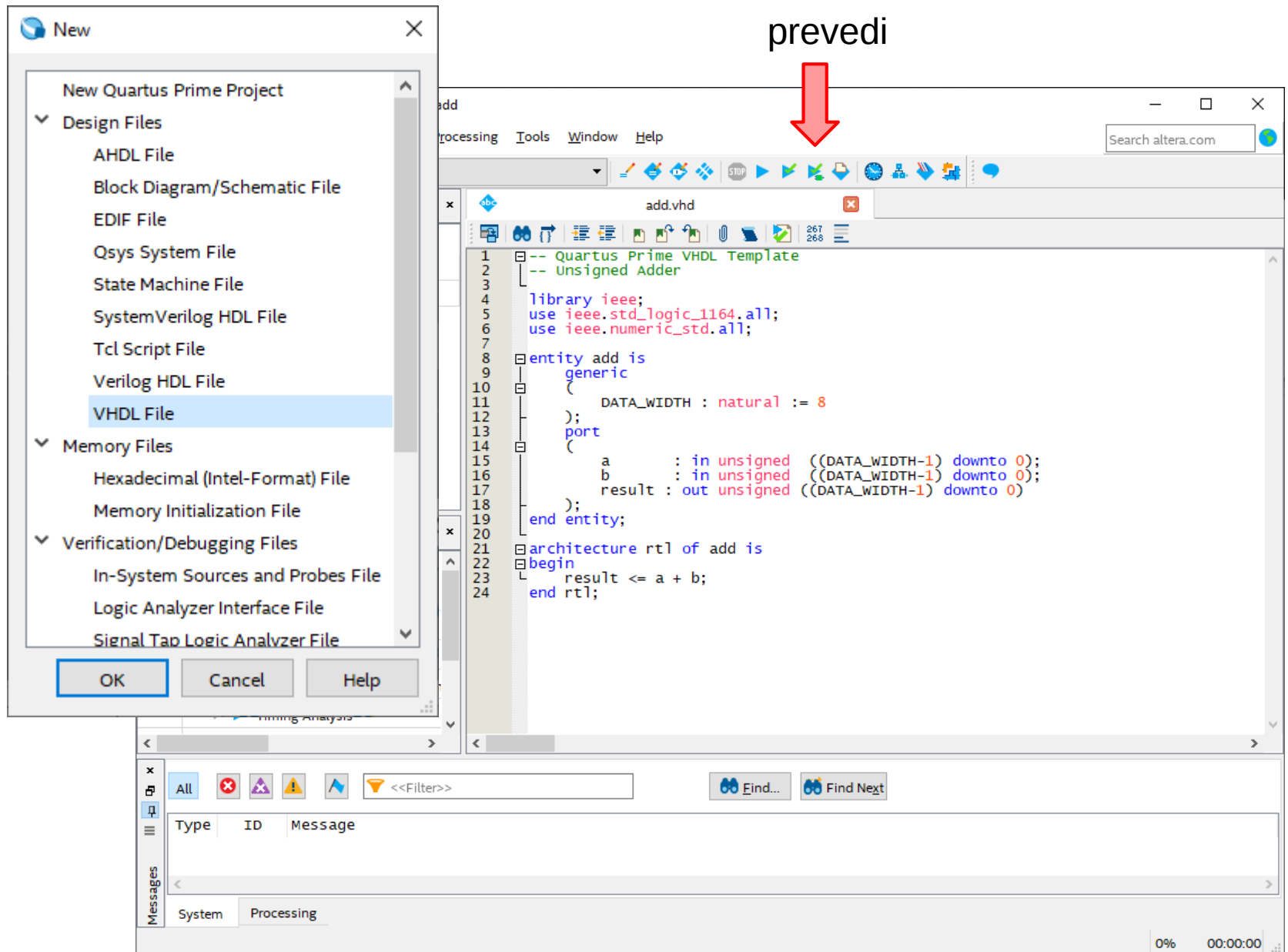


Zagon programa in odpiranje projekta



Opis vezja z enakim imenom, kot projekt

prevedi



The image shows the Quartus Prime IDE interface. On the left, the 'New' dialog box is open, displaying a list of file types under the 'Design Files' category. The 'VHDL File' option is selected. On the right, the 'add.vhd' file is open in the editor, showing a VHDL code snippet for an unsigned adder. A red arrow points from the word 'prevedi' (translate) to the top of the editor window. The code in the editor is as follows:

```
1  -- Quartus Prime VHDL Template
2  -- Unsigned Adder
3
4  library ieee;
5  use ieee.std_logic_1164.all;
6  use ieee.numeric_std.all;
7
8  entity add is
9      generic
10         (
11             DATA_WIDTH : natural := 8
12         );
13     port
14     (
15         a      : in unsigned ((DATA_WIDTH-1) downto 0);
16         b      : in unsigned ((DATA_WIDTH-1) downto 0);
17         result : out unsigned ((DATA_WIDTH-1) downto 0)
18     );
19 end entity;
20
21 architecture rtl of add is
22 begin
23     result <= a + b;
24 end rtl;
```

The bottom of the image shows the 'Messages' panel with tabs for 'System' and 'Processing'. The 'Processing' tab is active, and the status bar at the bottom right indicates 0% completion and a time of 00:00:00.

Pregled sheme sintetiziranega vezja

Quartus Prime Lite Edition - C:/MODB/add - add

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy

Entity: Instance

Cyclone IV E: AUTO

add

Table

Run Simulation Tool

Launch Simulation Library Compiler

Launch Design Space Explorer II

Timing Analyzer

Advisors

Chip Planner

Design Partition Planner

Netlist Viewers

RTL Viewer

Compilation Report - add

Summary

er>>

atus Successful - Mon Oct

Prime Version 20.1.0 Build 711 06/0

Name add

Entity Name add

Tasks Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate program)

Timing Analysis

RTL Viewer - C:/MODB/add - add

File Edit View Tools Window Help

Netlist Navigator

add

1'h0 CIN Add0

a[7..0] A[7..0]

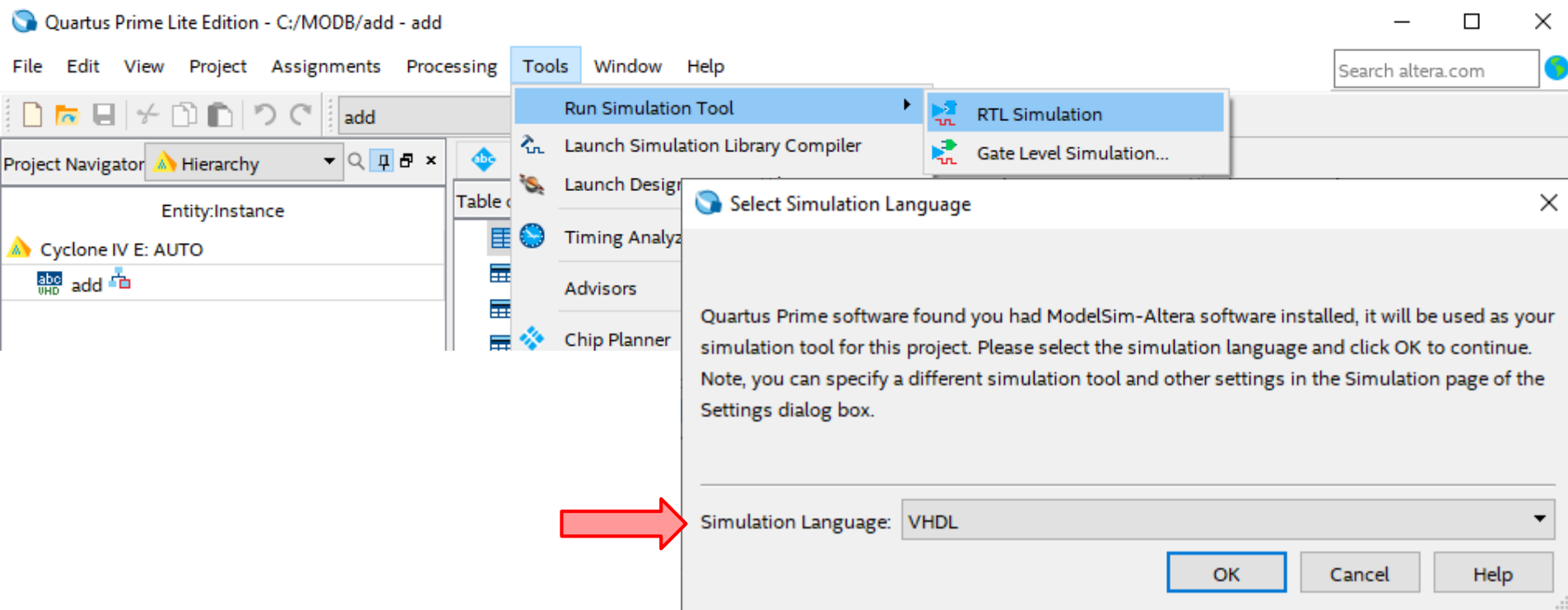
b[7..0] B[7..0]

OUT[7..0]

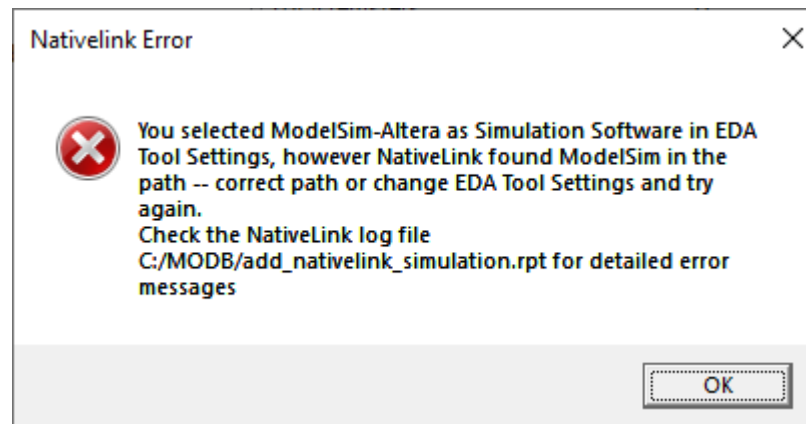
result[7..0]

100% 00:00:01

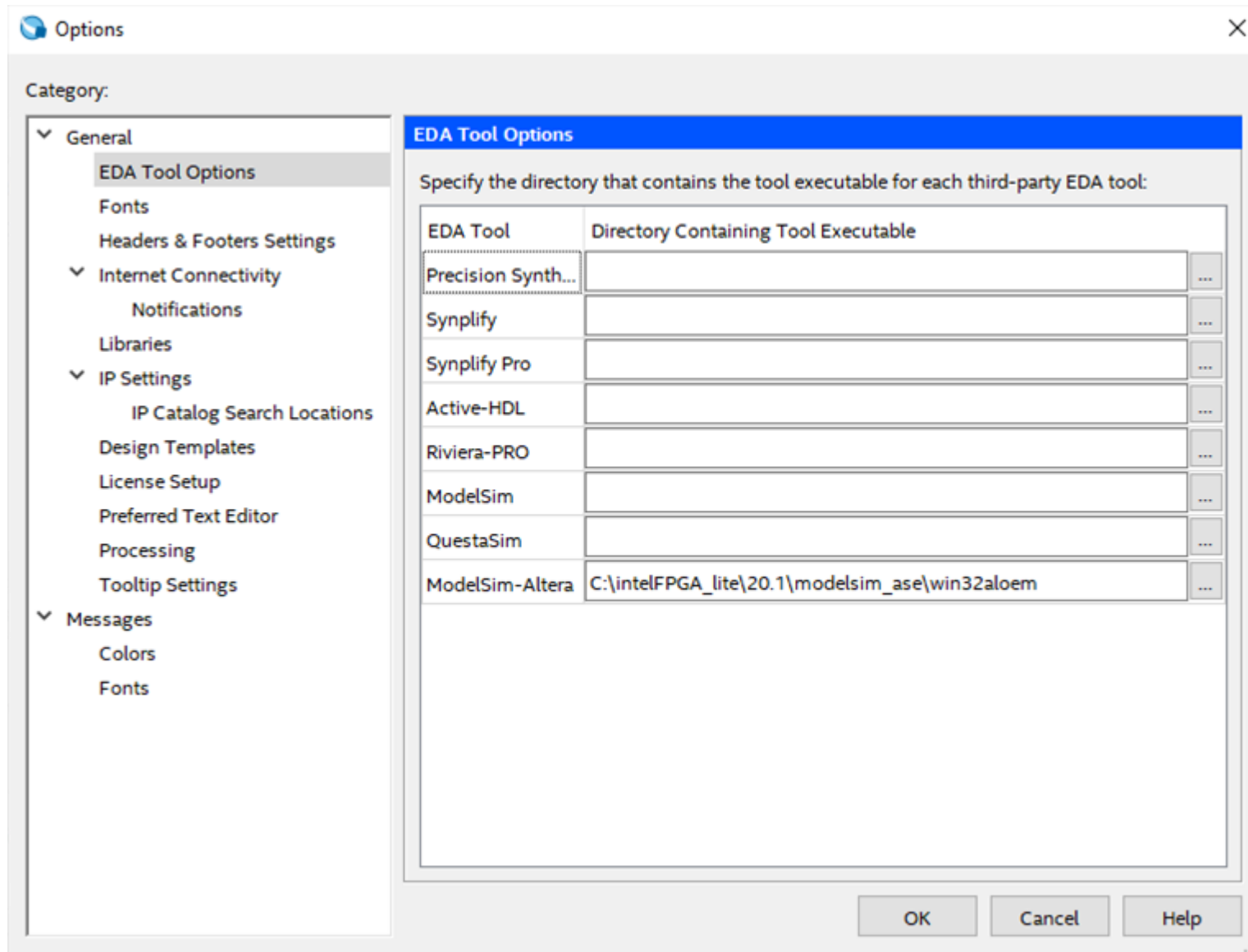
Simulacija z orodjem ModelSim



če dobimo to sporočilo,
moramo nastaviti poti
(naslednja stran)



Nastavitev Quartusa za uporabo ModelSim

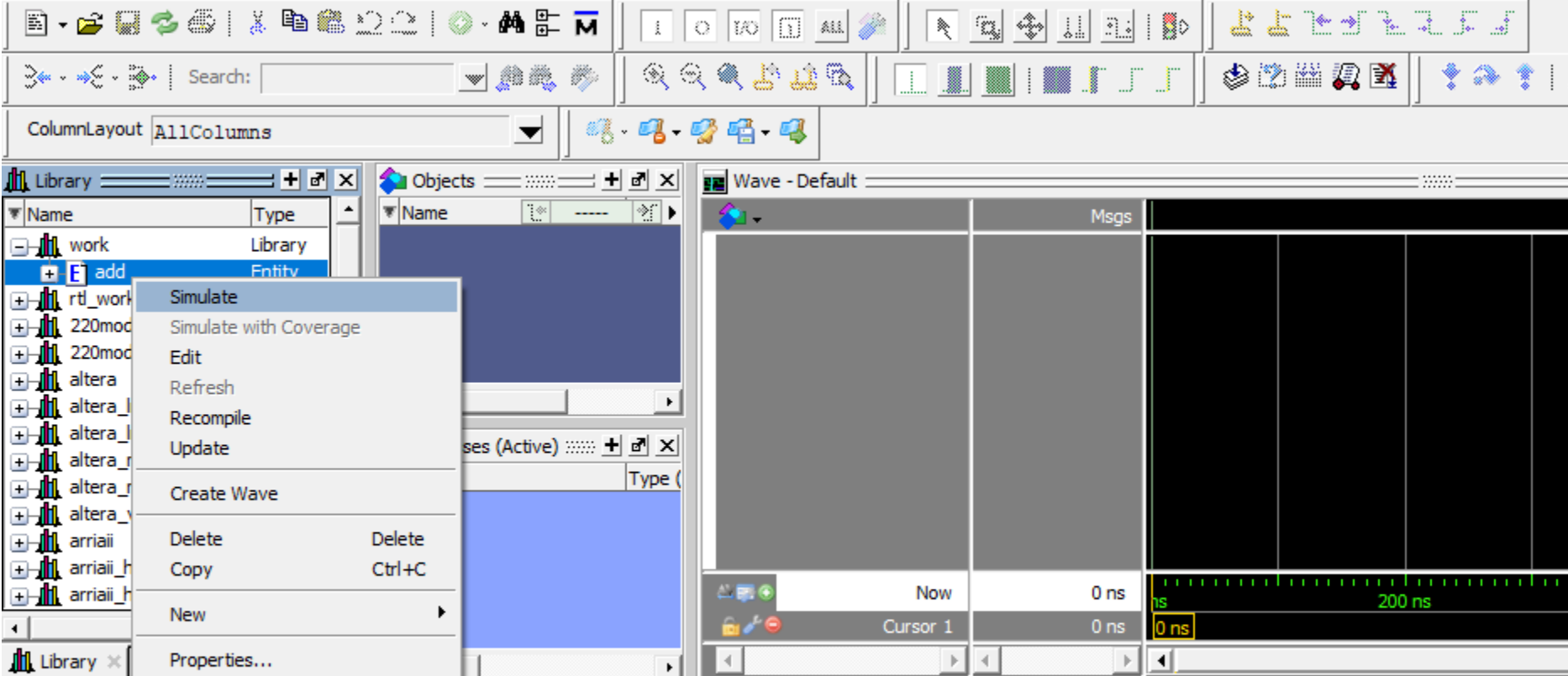


- ▶ V meniju Tools, Options nastavimo pot ModelSim-Altera

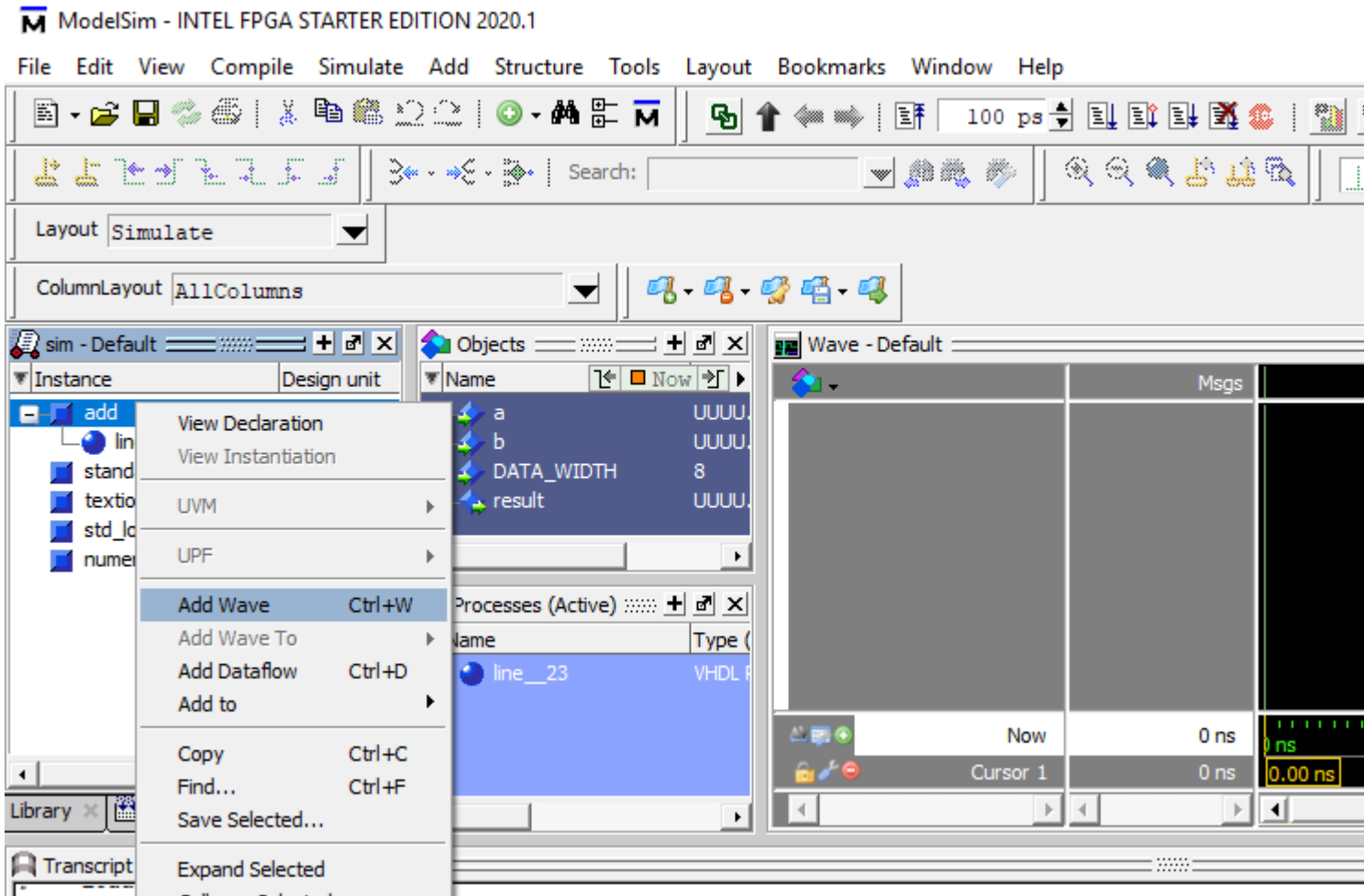
Start simulacije v ModelSim

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help



Določitev prikazanih signalov



- ▶ Add Wave doda vse signale, lahko jih pa nastavimo posamezno
 - ▶ levi klik na enega ali več signalov v Objects in prenos z miško v okno Wave

Nastavitev vhodov in simulacija

The screenshot displays the ModelSim software interface with the following components:

- Instance:** A tree view showing the design hierarchy. The 'add' instance is selected, showing its sub-components: 'line_23', 'standard', 'textio', 'std_logic_1164', and 'numeric_std'.
- Objects:** A list of objects in the simulation. The selected objects are 'a' (value 0000..), 'b' (value 0000..), 'DATA_WIDTH' (value 8), and 'result' (value 0000..).
- Processes (Active):** A list of active processes. The 'add' process is selected.
- Wave - Default:** A waveform viewer showing the simulation results. The selected waveforms are '/add/a', '/add/b', and '/add/result'. The waveforms show the values of these signals over time. The time scale is set to 0.1 ns, and the cursor is at 0.00 ns.
- Transcript:** A text window showing the simulation log. The log includes the following text:

```
# End time: 17:04:01 on Oct 05, 2020, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
#
ModelSim> vsim work.add
# vsim work.add
# Start time: 17:05:10 on Oct 05, 2020
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.add(rtl)
add wave -position insertpoint sim:/add/*
VSIM 4> force a 10#5
VSIM 5> force b 10#10
VSIM 6> run 100 ps
VSIM 7>]
```

► Navodila na:

<https://lniv.fe.uni-lj.si/altera/modelsim.htm>