Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

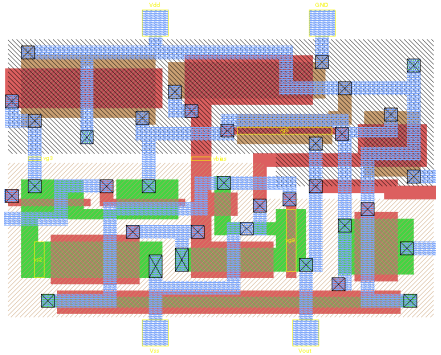
Uvod v laboratorijske vaje

Integrirana vezja
Načrtovanje digitalnih elektronskih sistemov

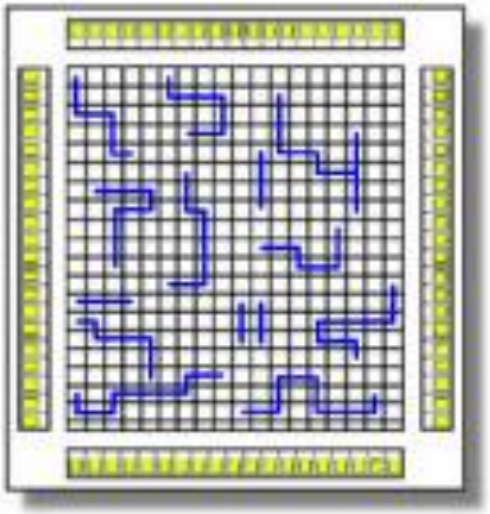
Literatura: A. Trost: Načrtovanje digitalnih vezij v jeziku VHDL, FE 2011

Digitalna integrirana vezja - tehnologija

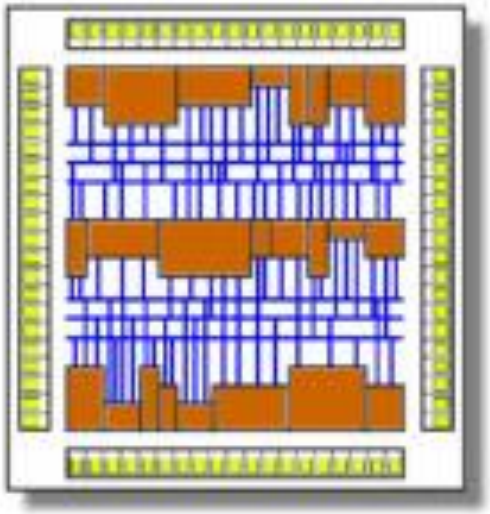
naročniška - Custom



Gate Array

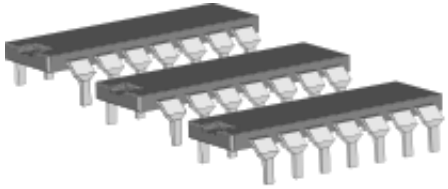


standardne celice

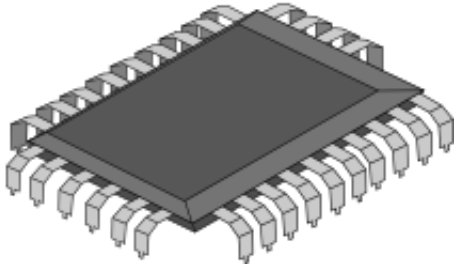


Digitalna integrirana vezja - funkcija

logični gradniki 74nn

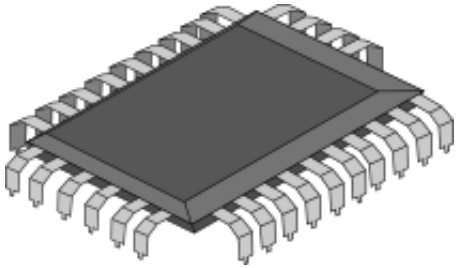


mikroprocesor



namensko vezje

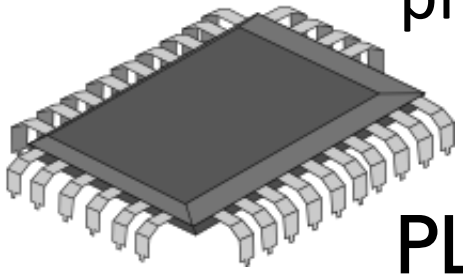
ASIC



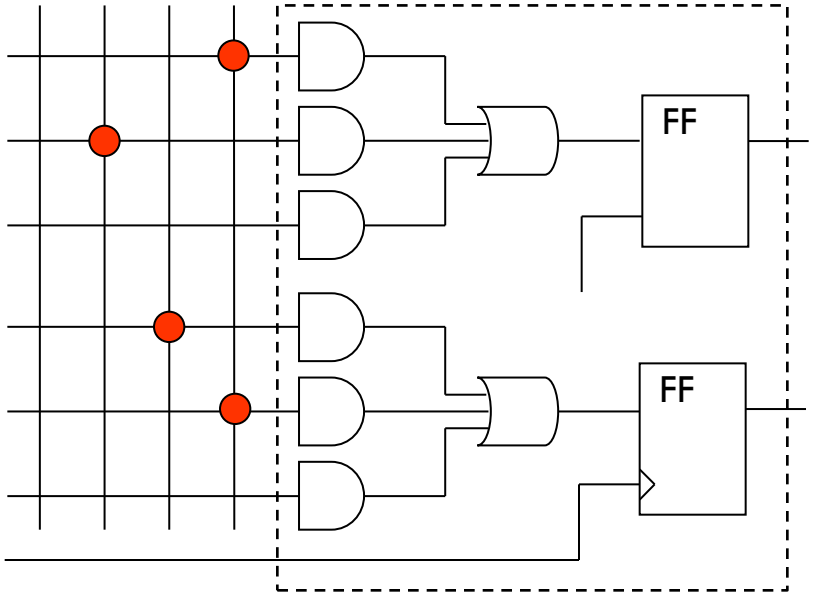
standardna vezja

?

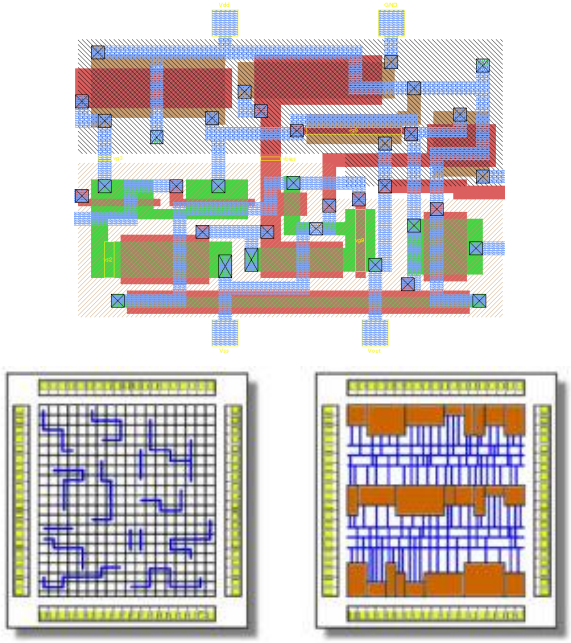
programirljivo integr. vezje

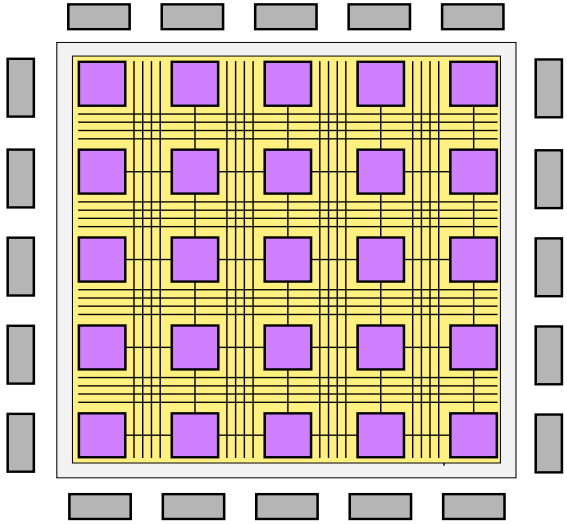


PLA



Programirljiva vezja FPGA

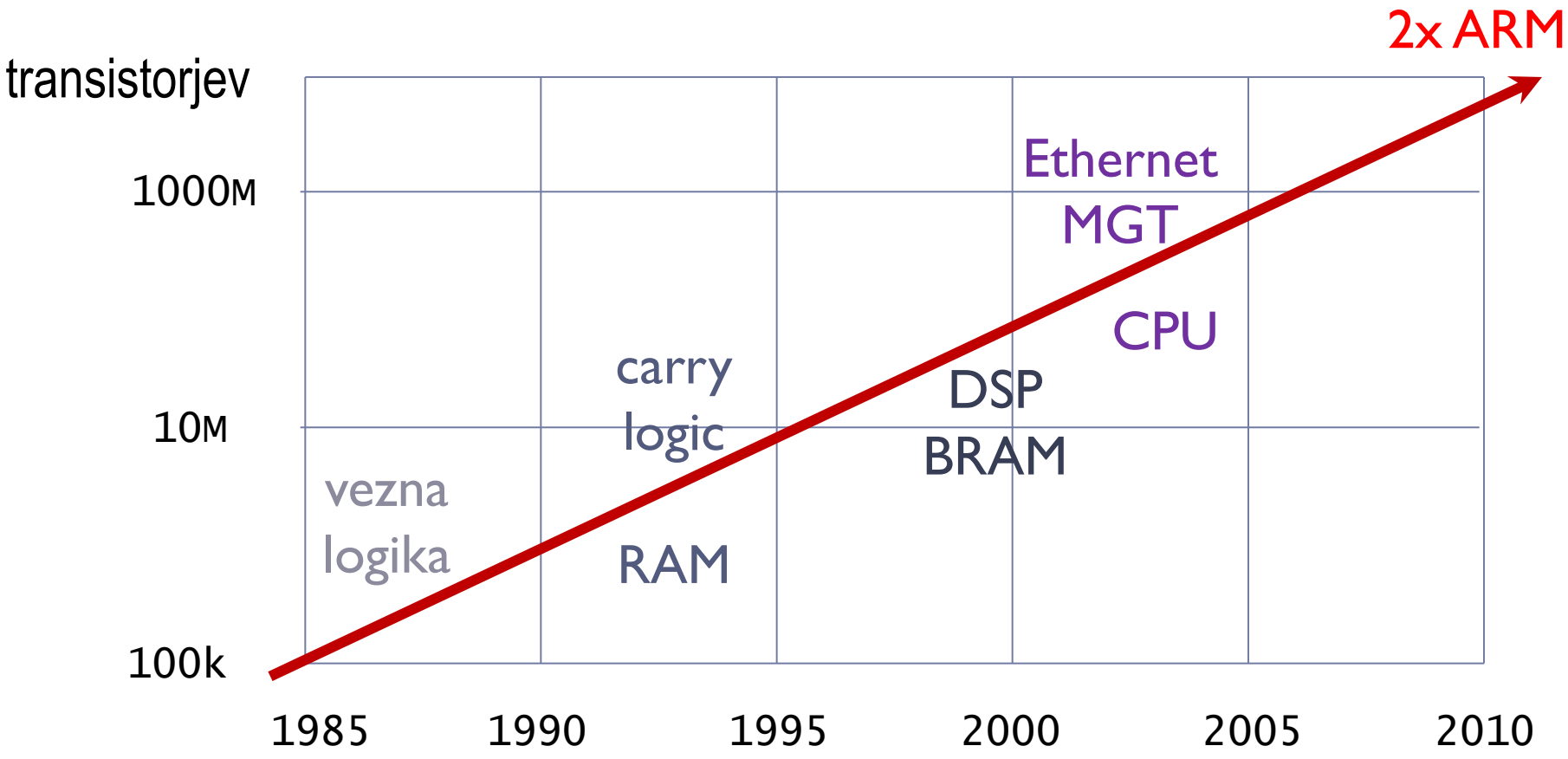




Field Programmable Gate Array

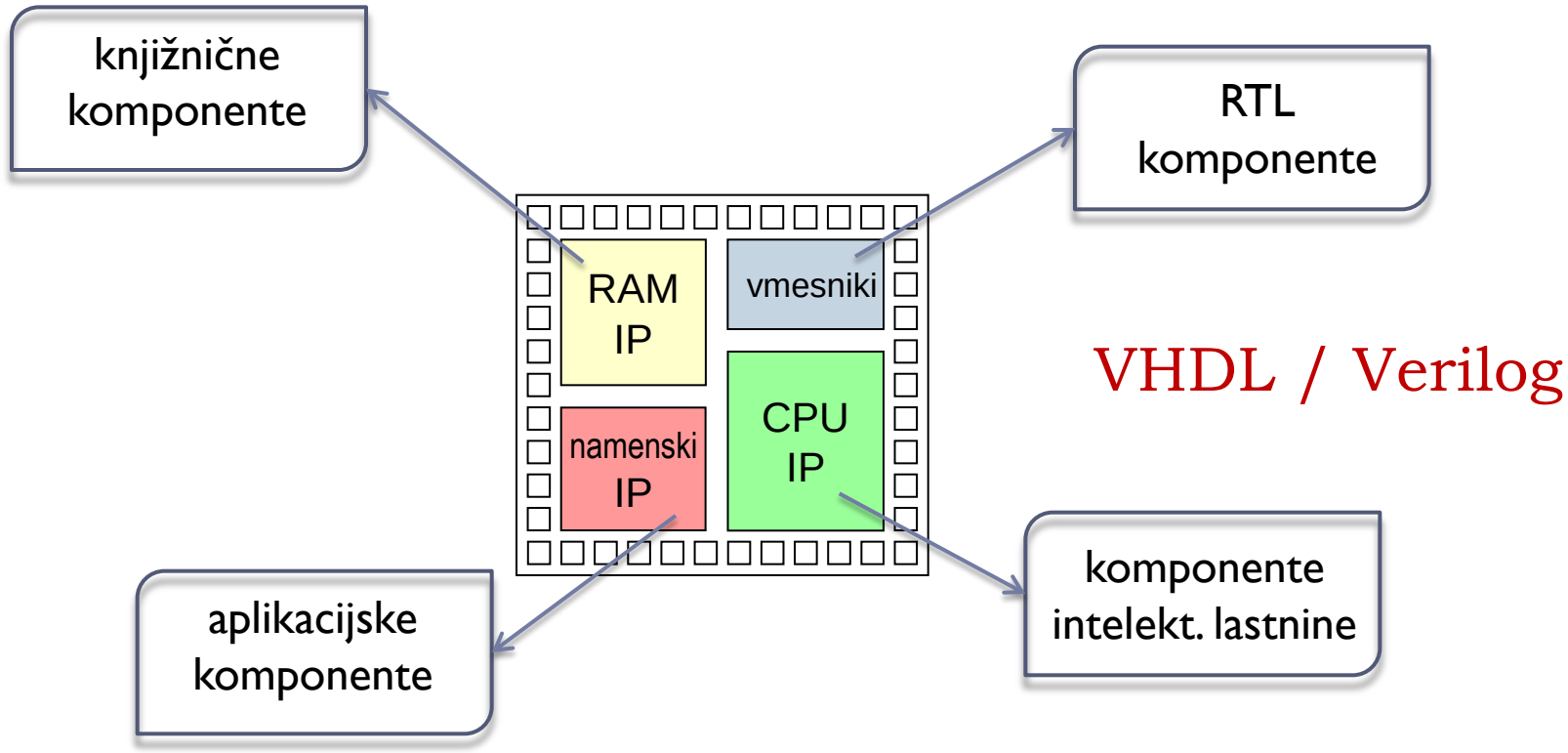
zmogljivost	stroški NRE	cena čipa	čas razvoja
ASIC	ASIC	FPGA	ASIC
FPGA	FPGA	procesor	FPGA
procesor	procesor	ASIC	procesor

Razvoj vezij FPGA

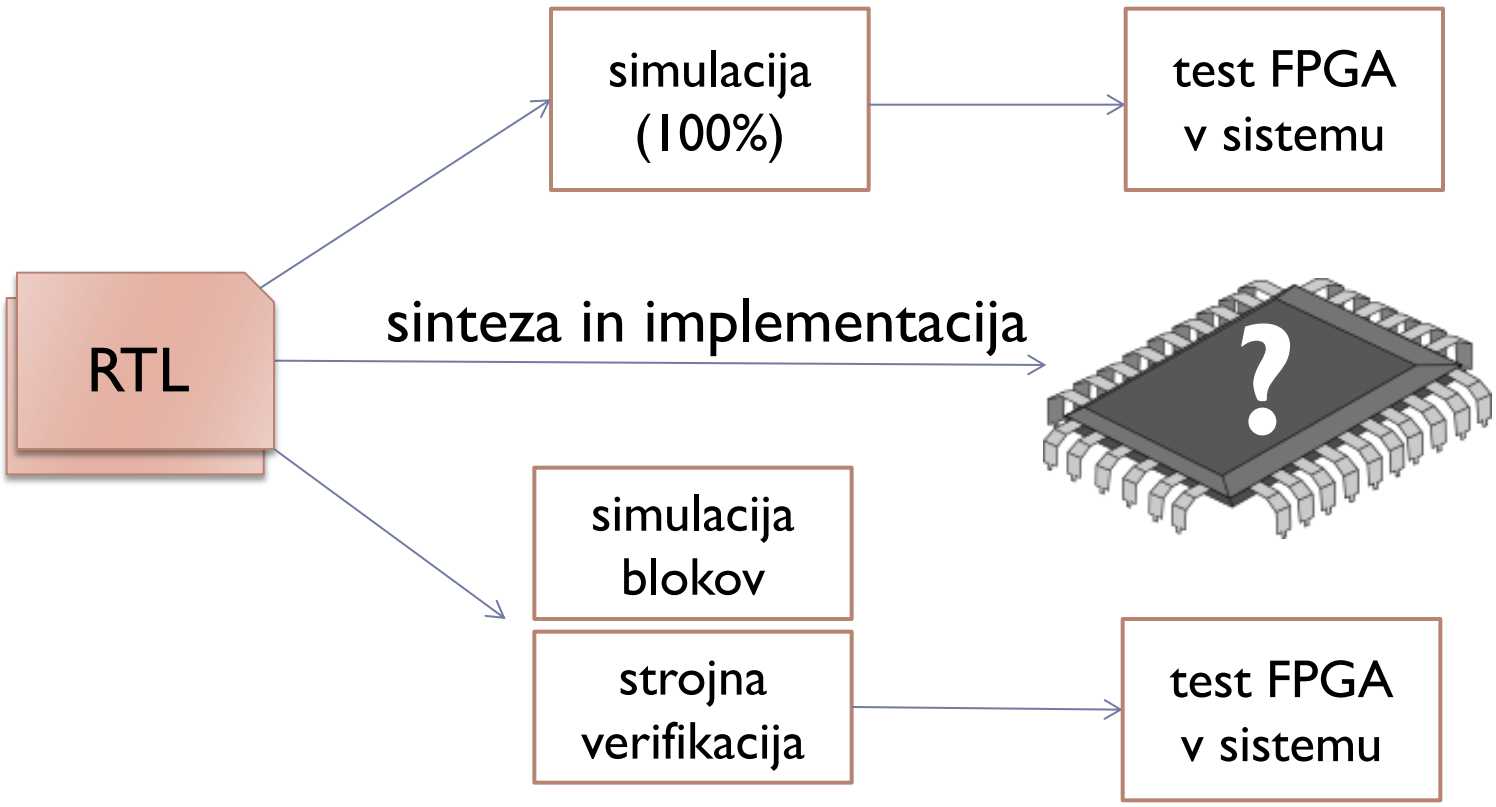


XILINX ALTERA LATTICE SEMICONDUCTOR Microsemi

Razvoj digitalnega vezja / sistema

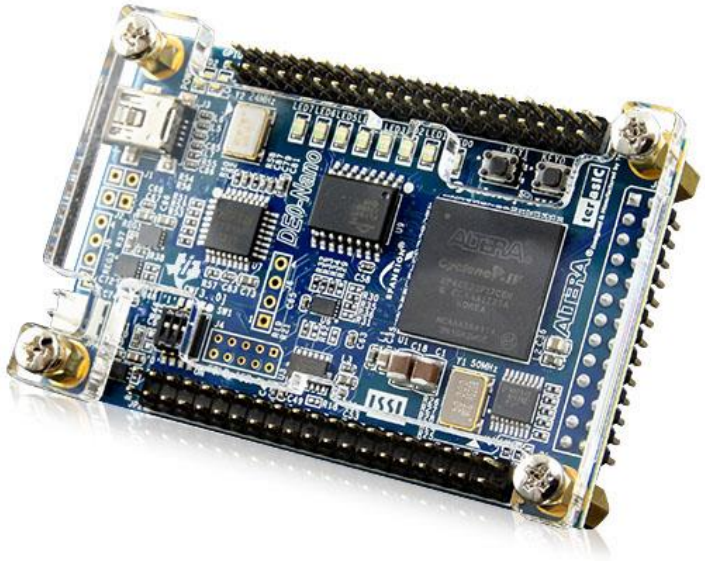


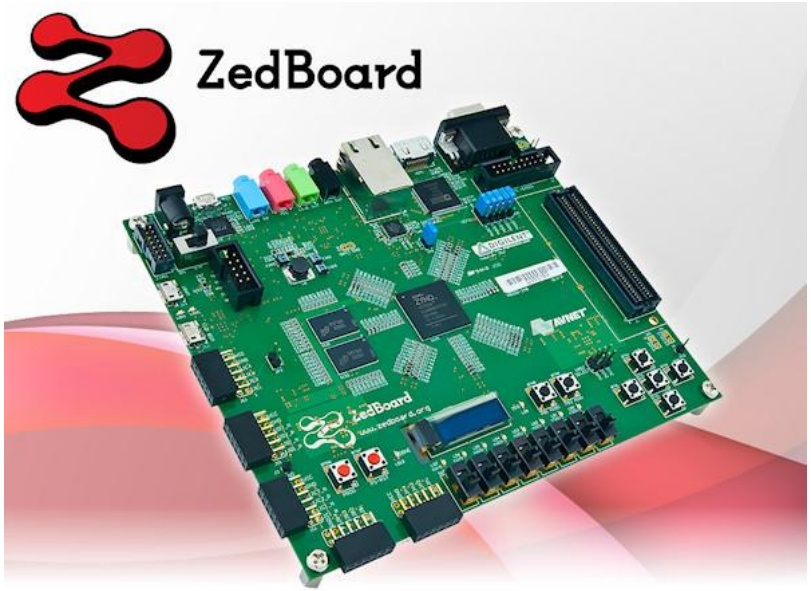
Verifikacija



FPGA razvojni sistemi

Altera DE0 Nano





Xilinx Zynq = FPGA+ARM

- http://lniv.fe.uni-lj.si/boards.html

Modul B: Vaje od števca do videoigre

1. strojne opreme
2. vmesniki
3. integracija in program