Digital Integrated Circuits and Systems

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Lab 5: square wave generator

Tool: Vivado 2025.1
Task: use binary counter and comparator to design square wave signal generator



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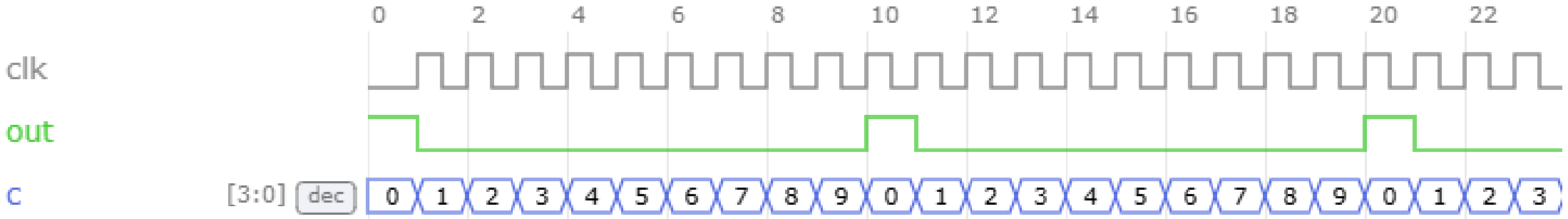
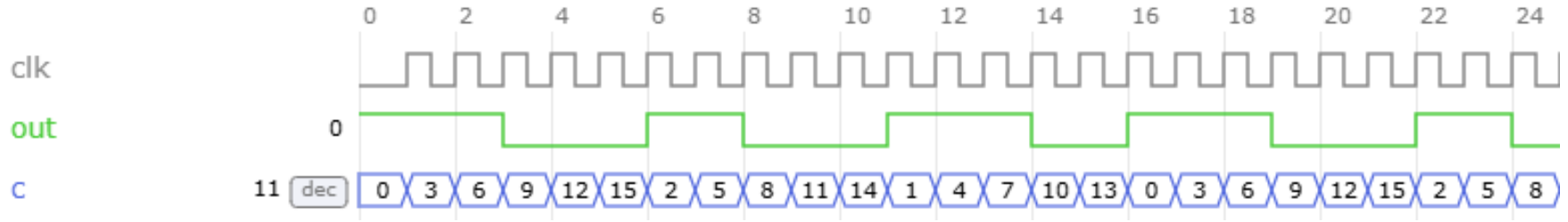
Counters for frequency division

- Design a 2-bit counter with logic output 1, when counter value is 0
  - Determine the frequency division ratio: f_{out} / f_{clk} = _____
  - Change to 4-bit counter and calculate: f_{out} / f_{clk} = _____
- Upgrade the 4-bit counter to count from 0 to 9 (modulo 10 counter) to achieve frequency division ratio 10.
- What is the main limitation of modulo counters for frequency division?



Accumulator

- Use a 4-bit counter as accumulator with specified increment
  - Counter should overflow (no reset condition)
  - Output is 1, when counter value is less than 8
- Determine division ratio with different increments



increment	f_{out} / f_{clk}	increment	f_{out} / f_{clk}
1		5	
2		6	
3		7	
4		8	

Square wave generator

- Design square wave generator with specified parameters:
  - f_{clk} = 125 MHz
  - min f_{out} = 10 Hz
- Calculate phase accumulator counter width: n = _____
- Calculate increments
  - f_{out} = 1 kHz increment = _____
  - f_{out} = _____ increment = _____
- Simulate your design in Vivado simulator