Digital Integrated Circuits and Systems

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Lab 4: N-bit averaging filter design and simulation

Tool: Vivado 2025.1
Task: design N-bit averaging filter, test on Vivado simulator and check circuit performance for selected N



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N-sample averaging filter

- Define N as a circuit parameter
  - N is constant value

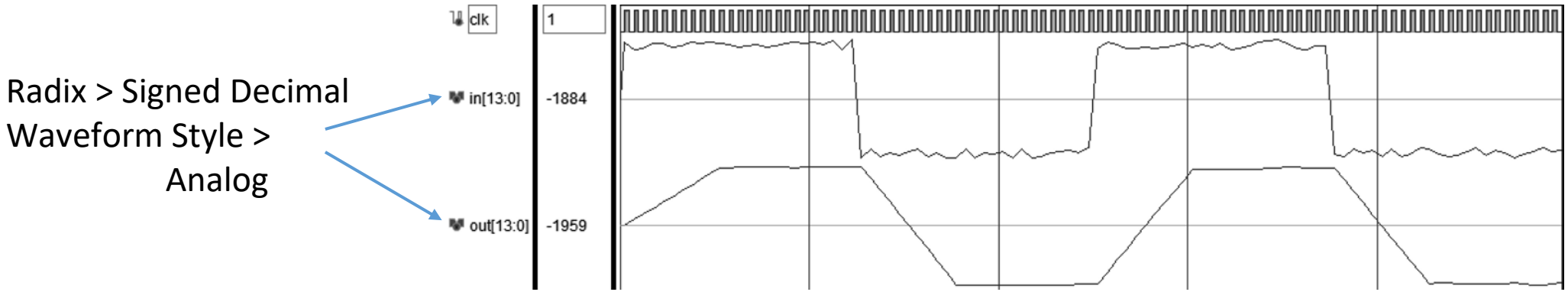
```
module avgN #(parameter int N = 10)(
  input logic clk,
  input logic signed [13:0] x,
  output logic signed [13:0] y
);
```

- Declare generic 14-bit array and logic vector for sum
- Use for loop to describe registers and compute running sum
  - add current input and subtract the oldest data
- Use division operator for output

```
logic signed [13:0] z [N];
...
always_ff @(posedge clk) begin
 z[0] <= x;
 for (int i = 1; i < N; i++) begin
  z[i] <= z[i-1];
 end
 sum <= sum + x - z[N-1];
 y <= ...
end
```

Simulate and check performance

- Simulate using online simulator
- Add circuit to Vivado project, check elaborated schematic
- Simulate in Vivado with the provided testbench, explain result



- Synthesize, Implement and analyze the circuit performance

circuit	LUT / FF / DSP	Data Path Delay [ns]	Logic levels	clk period [ns]	frequency [MHz]