Digital Integrated Circuits and Systems

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Lab 2: Registers and arithmetic operations in FPGA

Tool: Vivado 2025.1
Task: design a circuit model for basic operations, run synthesis, analyze utilization and timing performance

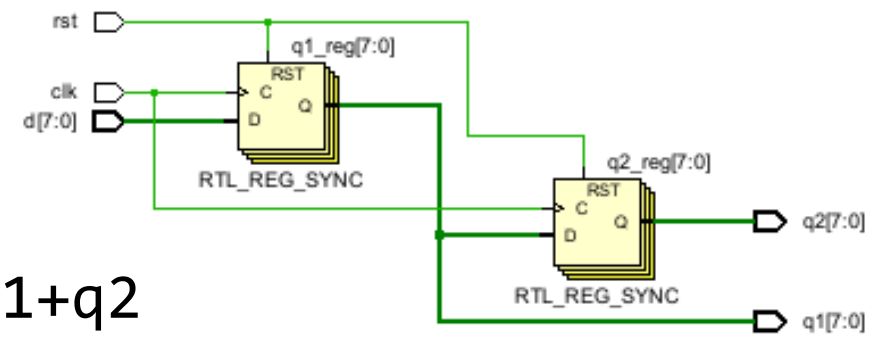




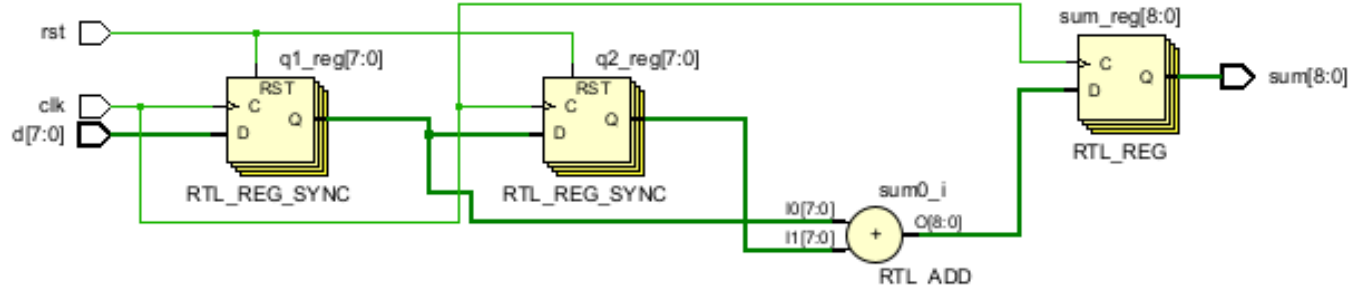
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Simulate registers

1. Open SystemVerilog educational simulator https://lniv.fe.uni-lj.si/svlog/
   - Basics: sequential logic, example: Register
   - simulate circuit with one 8-bit register
2. Use Vivado to check elaborated schematic
3. Modify circuit to include two registers: q1, q2
   - check with simulator and elaborated schematic



4. Add q1 and q2 to produce 9-bit sum: `sum = q1+q2`
   - check the difference if sum is inside or outside **always_ff** block



NOTE: Assignment in block **always_ff** describes registers!

Analyze circuit performance in FPGA

1. Add Vivado constraints: clk period 10 ns
   - PROJECT MANAGER, Add Sources, Add or create constraints

```
create_clock -name clk -period 10.000 [get_ports clk];
```

2. Run Synthesis, Run Implementation
   - Check reports:
     - Design Runs: read number of LUT and FF
     - Project Summary: read Timing WNS
     - Calculate: Min clock period = 10 ns - WNS and frequency

Utilization of LUTs	Number of flip-flops (FF)	Min clk period [ns]	Frequency [MHz]

```
module reg_sum (
  input  logic clk, rst,
  input  logic [7:0] d,
  output logic [8:0] sum
);

logic [7:0] q1, q2;

always_ff @(posedge clk) begin
 if (rst) begin
    q1 <= '0;
    q2 <= '0;
 end else begin
    q1 <= d;
    q2 <= q1;
 end
 sum <= q1+q2;
end

endmodule
```

Analyze registered operations (sum, multiply, divide)

circuit	Utilization LUT	Utilization FF	Utilization DSP	clk period [ns]	frequency [MHz]
add 14					
add 28					
mul 14					
mul 28					
div 14					
div 28					

Background and Outcomes

- Understand SystemVerilog models with operators and registers
- Use Vivado for design and synthesis
- Analyze FPGA utilization and delay
- Understand implementation cost of basic arithmetic operations

Prerequisites

- SystemVerilog and digital circuit fundamentals

https://lniv.fe.uni-lj.si/svlog/fundamentals.html

- Basic understanding of FPGA structure and design flow