Digital Integrated Circuits and Systems

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Lab 8: FIR filter on Red Pitaya

Tool: Vitis 2025.1, Vivado 2025.1
Task: Compile and test applications project on Red Pitaya board, insert your FIR filter and test operation on the board

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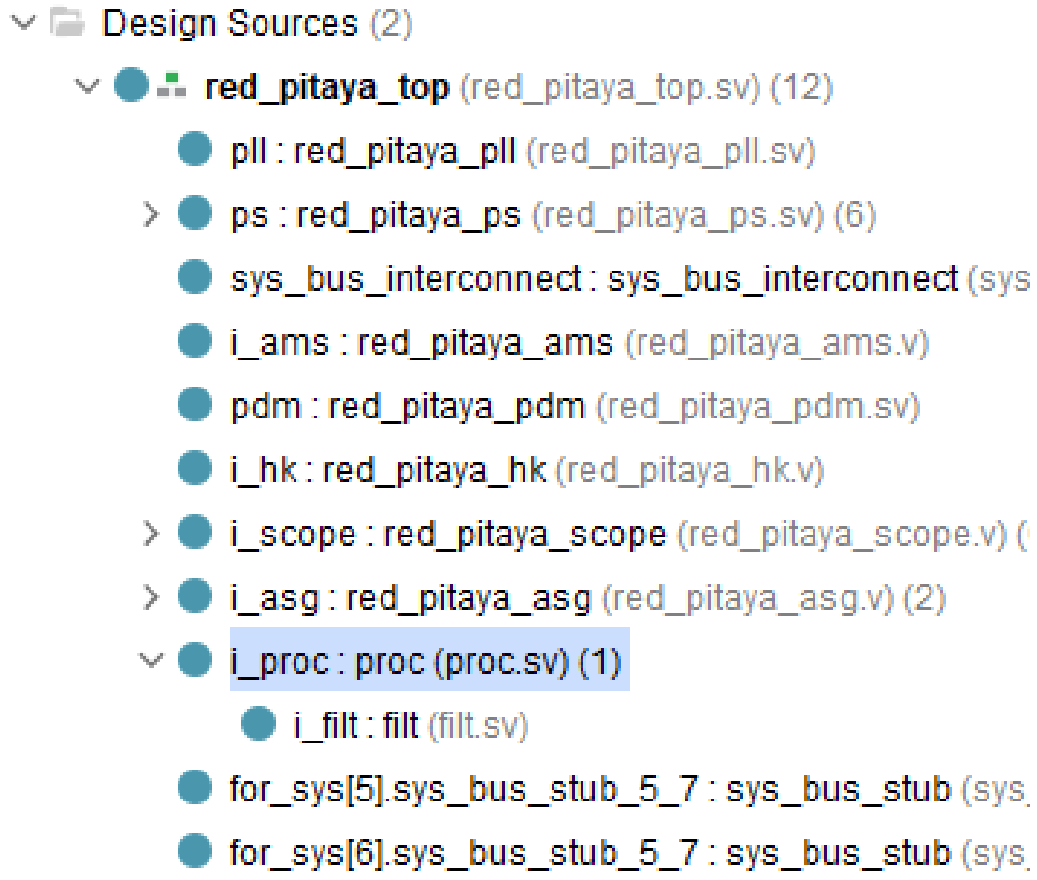
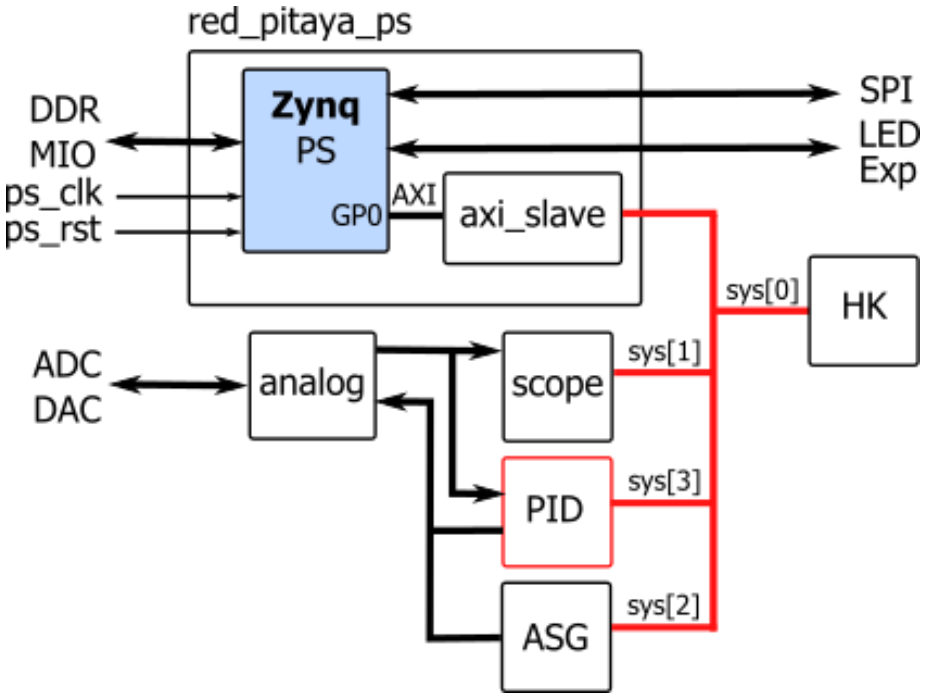
Red Pitaya STEMlab board

- FPGA development board for test and measurement
- two 125 MHz analog inputs and outputs
- System-on-chip with FPGA and ARM CPU running Linux
- connect to PC for user interface
  - e.g. applications in web browser

Red Pitaya applications project

- Vivado project: lniv.fe.uni-lj.si/courses/div/RP25a.7z
  - logic for digital oscilloscope, signal generator...
  - replaced PID with signal processing component





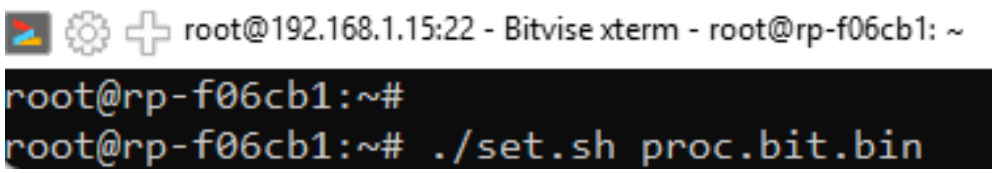
Generate bitstream and upload to Red Pitaya

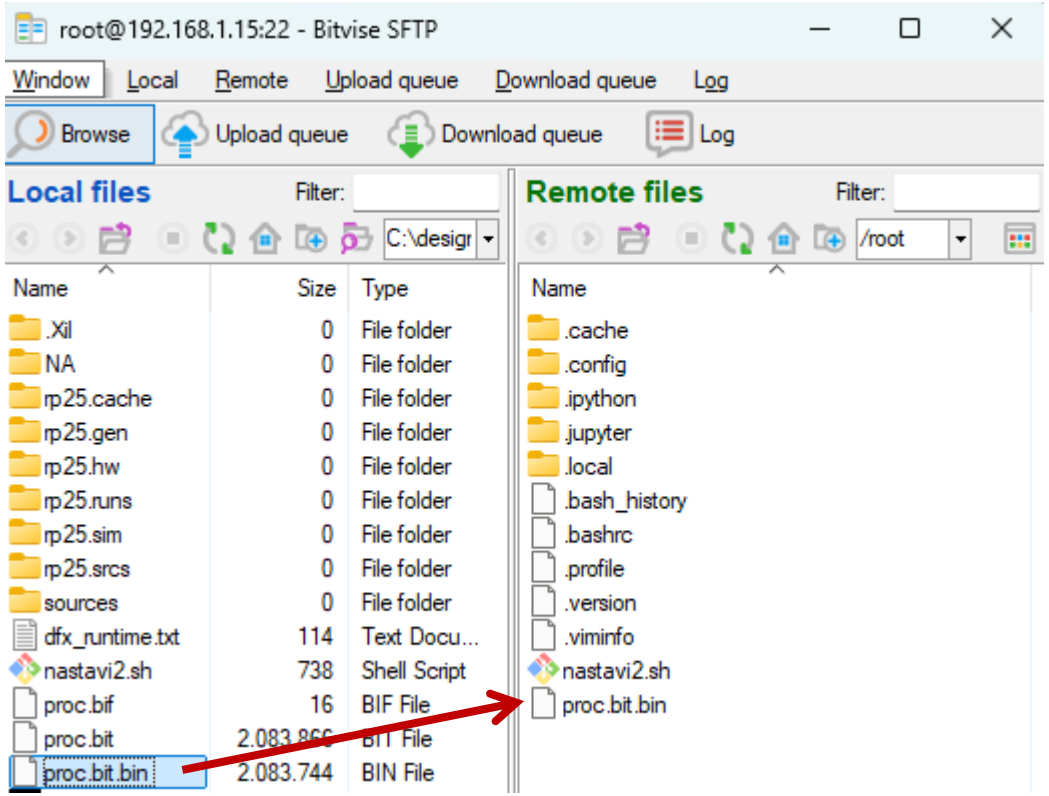
- Compile: Run Synthesis, Run Implementation, Generate Bitstream
- Format FPGA config file in Tcl Console x

```
cd c:/proj/rp25a
source ./format.tcl
```

- Run Bitvise SSH Client
  - Log in
  - New SFTP window, upload proc.bit.bin
  - New terminal, set your FPGA config file

```
./set.sh proc.bit.bin
```



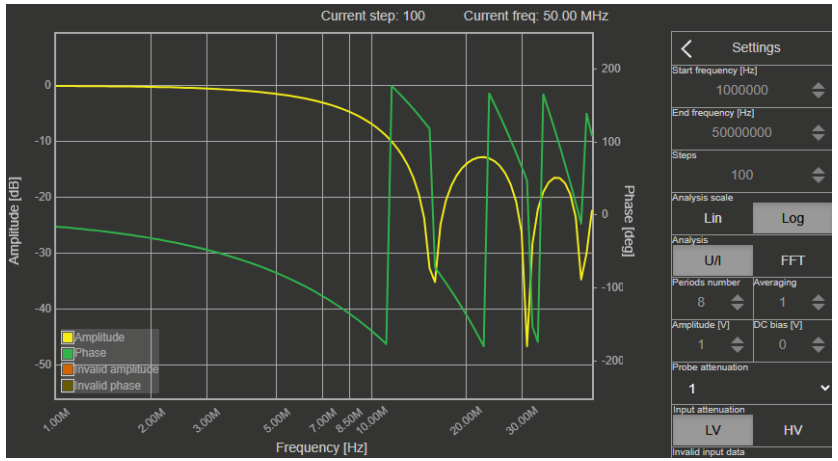


Test with applications

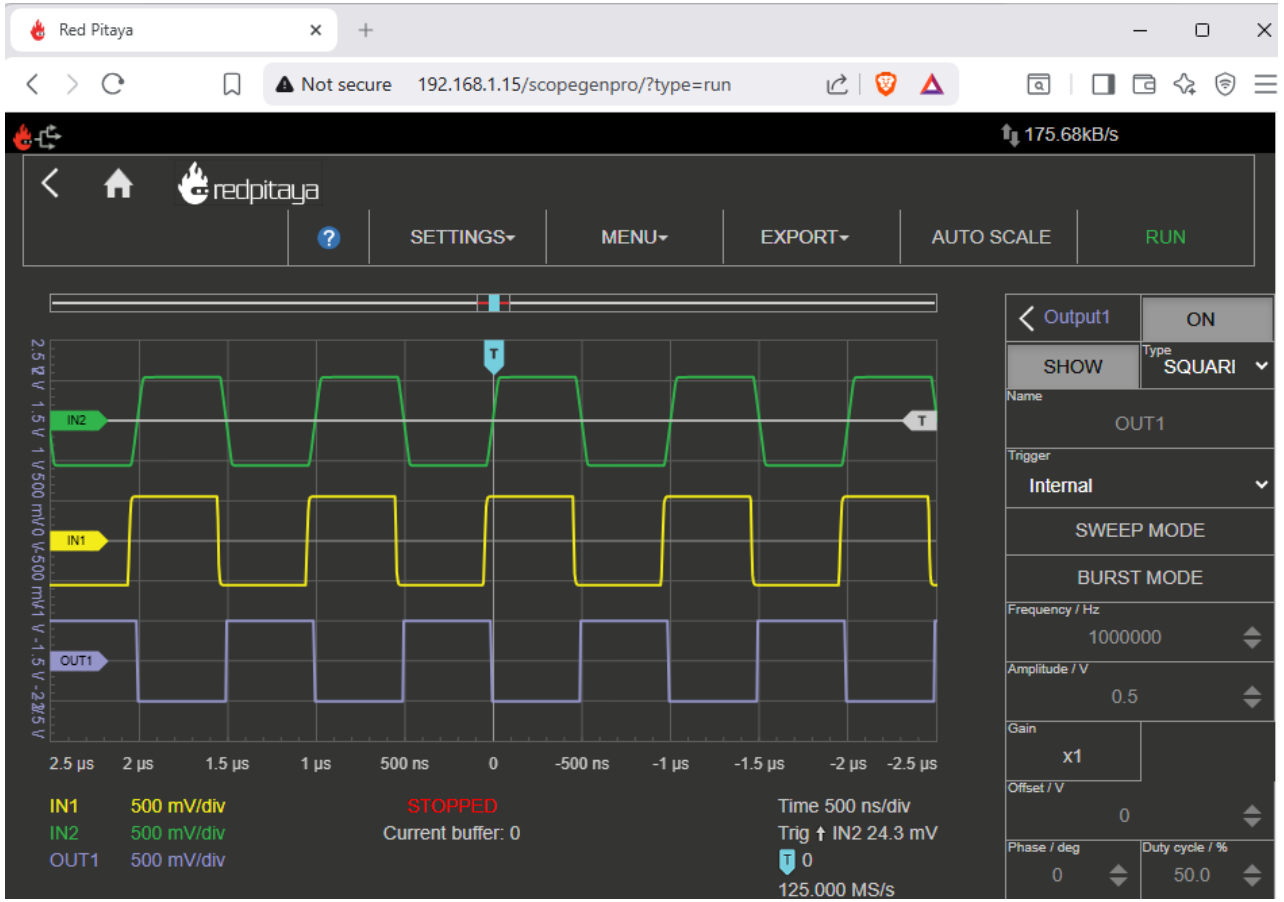
- Web browser: 192.168.1.15, run Oscilloscope application and test filter
- set OUT1: Square, 1 MHz, show IN1 and IN2 (IN2 is filtered signal)

- run Bode Analyser application
- set Start: 1MHz, End: 50 MHz, 100 steps

-20 dB=1/10
-40 dB=1/100

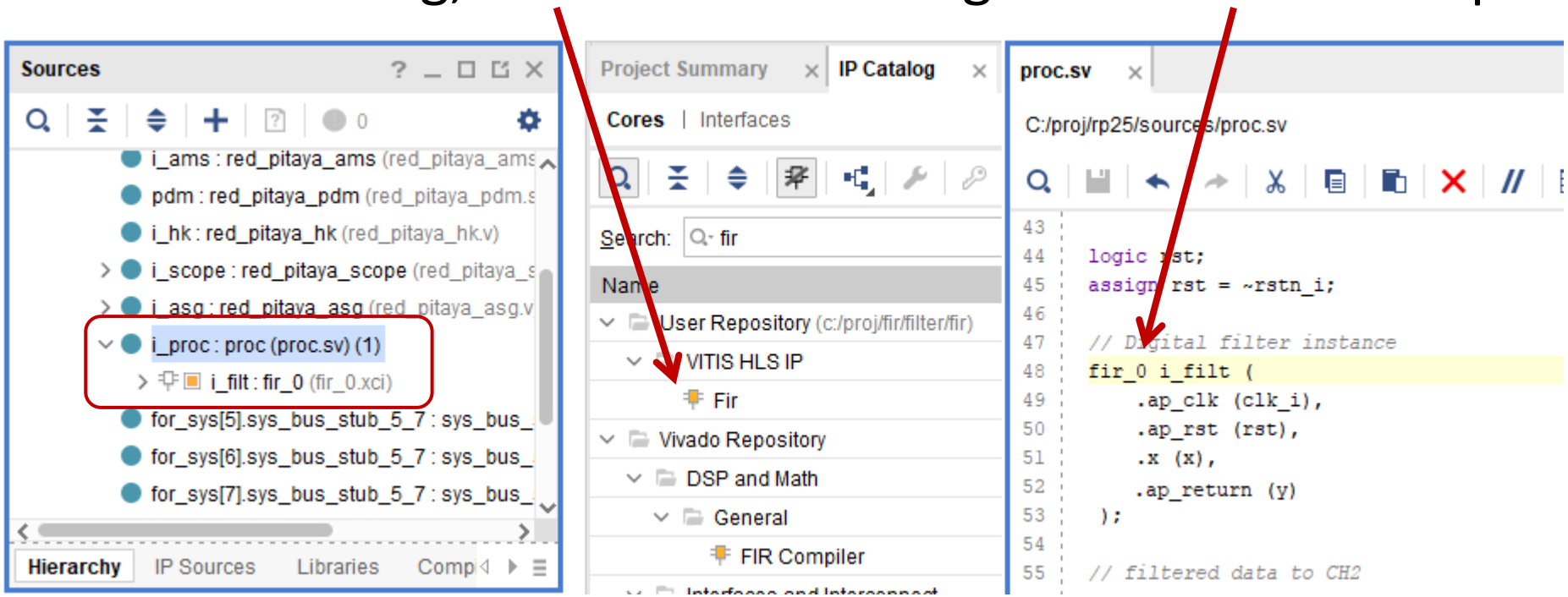


yellow plot is averaging filter response



Test your FIR

- Add your IP from Vitis into IP Catalog of Vivado Red Pitaya project
- Search IP Catalog, add filter and change module name in proc.sv



- Repeat the steps to compile project, format, upload and test on board !