Digital Integrated Circuits and Systems

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Lab 5: Digital filter with HLS

Tool: Vitis 2025.1
Task: Describe in C++ and synthesize digital averaging filter, extend to N-tap filter, simulate and synthesize with directives.

Filter for computing average of two samples

- fixed point data in range -1 .. +1
- store old input values in a static variable
- Your task:
  - compute average of current and last sample
  - save input value for the next function call
  - add main function (testbench) and simulate
  - run synthesis

```
#include <ap_int.h>
#include <iostream>

#define DT ap_fixed<10,1>

DT filt(DT x)
{
 static DT x1 = 0;
 DT r;
 ...
 return r;
}
```

latency cycles	interval cycles	LUT / FF / DSP

```
int main() {
 DT x[] = {0, 0.1, 0.3, 0.5};

 for (int i = 0; i < 4; i++) {
   DT y = filt(x[i]);
   std::cout << "x=" << (float)x[i]
   << " y=" << (float)y << "\n";
 }

 return 0;
}
```

Explore and extend filter model

- effect of fixed data size to representation of real values
  - simulate and observe values for 5, 10, 15 and 20 bits
- extend code to compute average of 3 samples
  - store last 2 values: x2 = x1; x1 = x;
- determine correct data format for sum to prevent overflow

```
DT ap_fixed<10,1>

SUMT ap_fixed<___, __>
```

- run sythesis

latency cycles	interval cycles	LUT / FF / DSP

N-tap filter

- design 7-tap averaging filter
  - declare static array
  - write a delay loop: z[6] = z[5]; z[5] = z[4];… z[0] = x
  - send oldest value to output and test delay loop on simulation
- add summation loop
  - determine appropriate sum data format
- verify on simulation and run synthesis

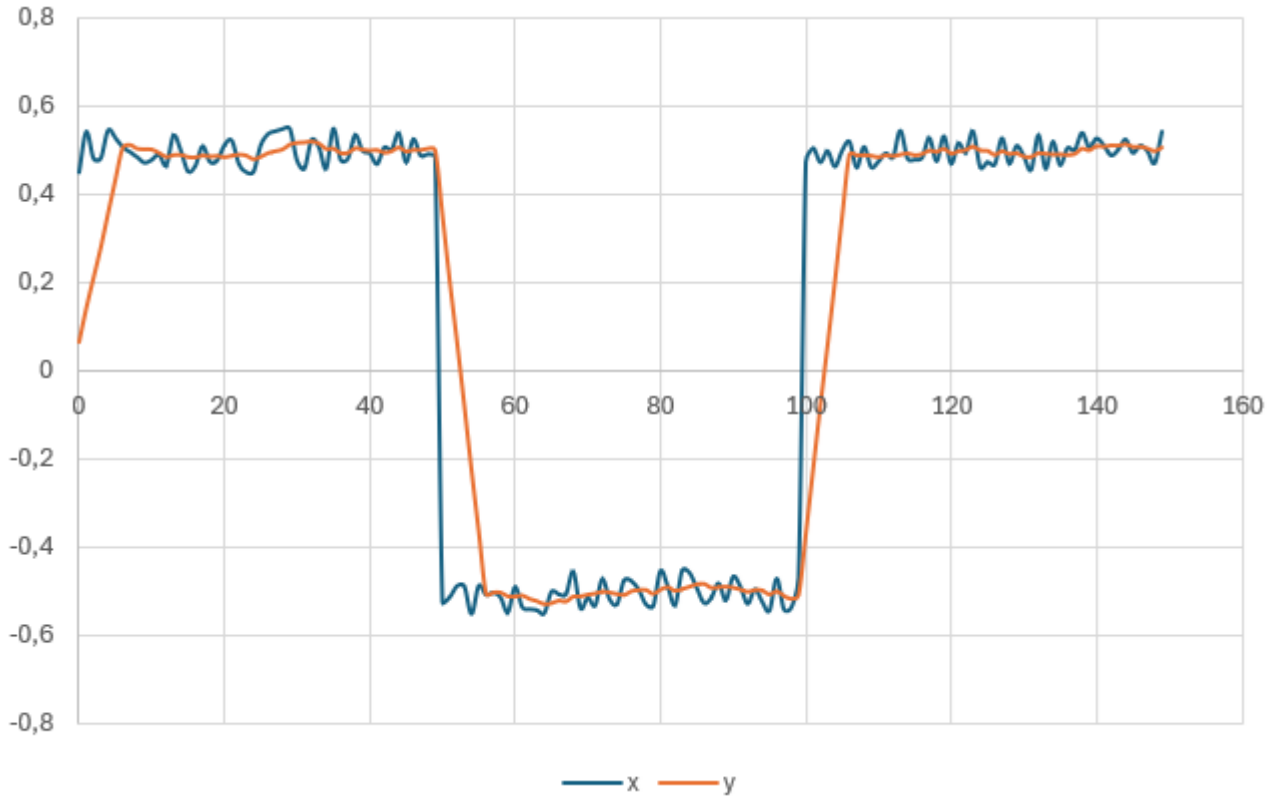
```
static DT z[7];

for (int i= ... ) z[i]=z[i-1];
z[0] = x;
```

latency cycles	interval cycles	LUT / FF / DSP

Simulation of N-tap filter

- Use provided testbench for simulation
  - comment existing main() function
  - add testbench file
  - run simulation
  - open output file in Excel and draw scatter data plot



Optimize synthesis

- filter performance with different directives
  - Unroll delay loop
  - Unroll summation loop
  - Pipeline complete function

circuit	clock [MHz]	latency cycles	interval cycles	LUT / FF / DSP

- Is it possible to synthesize N-tap filter with parameter N?
  - explore synthesis and directives...