Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

Preizkušanje elektronskih vezij

Design for Testability
Načrtovanje za testiranje

Overview

- Introduction
- Testability Analysis
- Design for Testability Basics
- Scan Cell Designs
- Scan Architectures
- Scan Design Rules

Ad Hoc Approaches

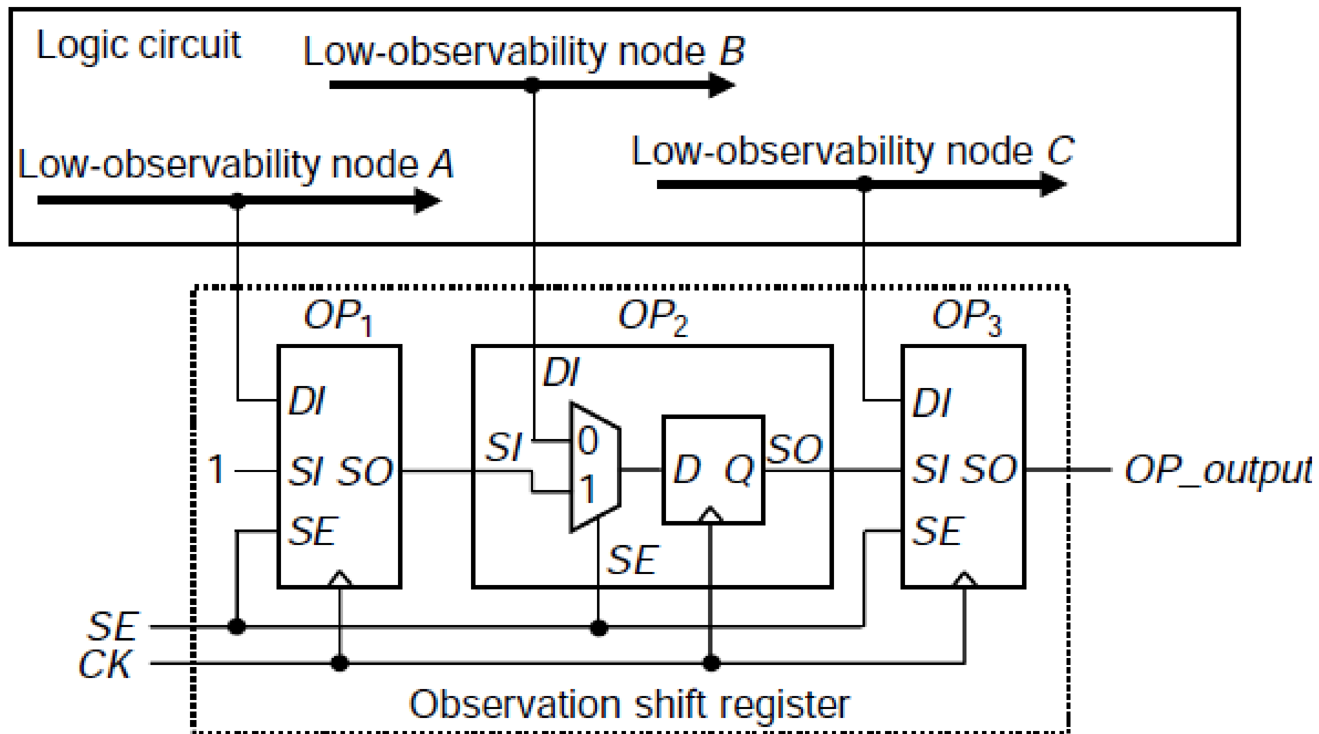
- Non-systematic approach for improving testability.
- These techniques are not methodological -- have to be repeated differently on new designs.
- The most common used ad hod approaches are:
  - Test point insertion
  - Avoiding combinational feedback loops
  - Avoiding redundant logic
  - Partitioning large circuit into small blacks

Test Point Insertion (TPI)

- DFT technique for the controllability and observability of internal nodes.
- Testability analysis is typically used to identify the internal nodes where test points should be inserted.
- Example of observation point insertion for a logic circuit with 3 low-observability nodes.

Test Point Insertion - Observability

- OP_2 shows a structure of an observation point (*OP*) that is composed of a multiplexer (MUX) and D flip-flop.



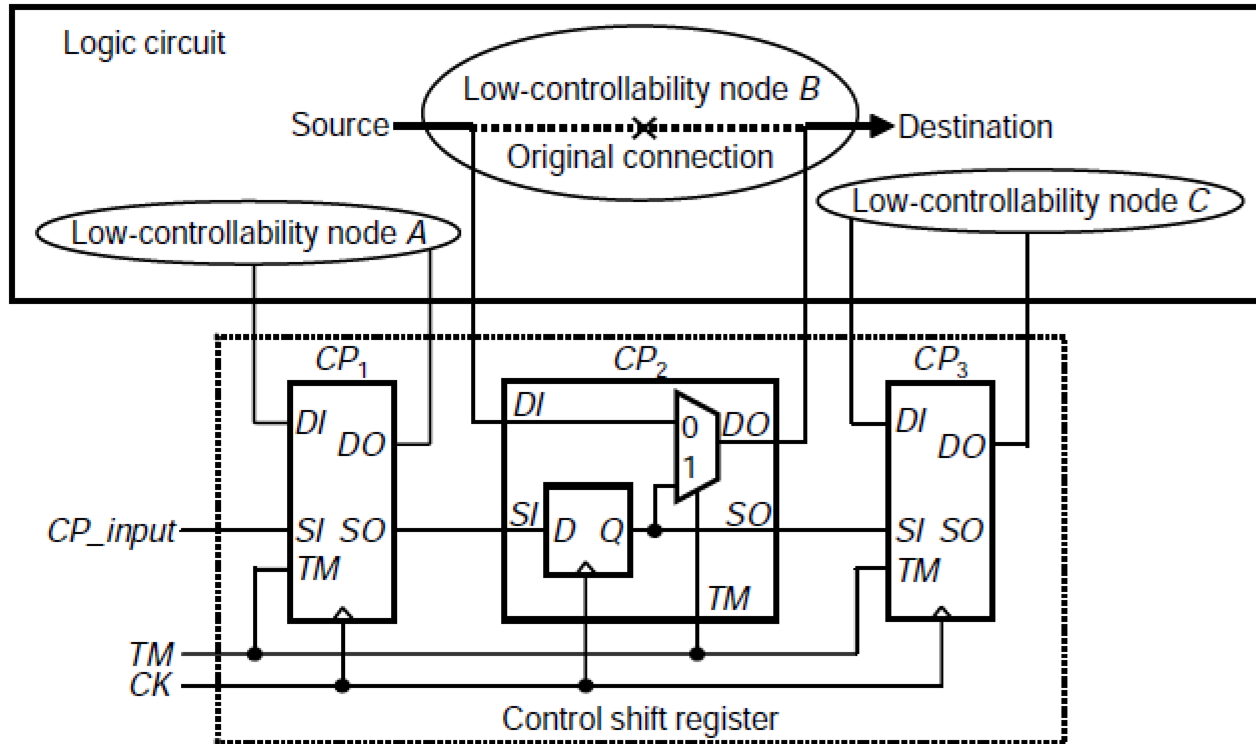
Test Point Insertion - Observability

- When *SE* = 0 and the clock *CK* is applied, the logic values of the low-observability nodes are captured into the D flip-flops.
- When *SE* = 1, the D flip-flops within OP_1, OP_2 and OP_3 operate as a shift register, allowing us to observe the captured logic values through *OP_output* during sequential clock cycles.
- As a result, the observability of the circuit nodes is greatly improved.

Test Point Insertion - Controllability

- Example of control point insertion for a logic circuit with three low-controllability nodes.
- CP_2 shows the structure of a control point (*CP*) that is composed of a multiplexer (MUX) and D flip-flop.
- The original connection at a low-controllability node is cut and a MUX is inserted between the source and destination nodes.
- During normal operation, the test mode (TM) is set to 0, so the value from the source node drives the destination node through the 0 port of the MUX.

Test Point Insertion - Controllability



Test Point Insertion - Controllability

- During the test, TM is set to 1 so that the value from the D flip-flop drives the destination node through the 1 port of the MUX.
- D flip-flops in OP_1, OP_2 and OP_3 form a shift register, so the required values can be shifted into the flip-flops through CP_input and used to control the destination node of low-controllability nodes.
- As a result, controllability of the internal circuit node is significantly improved.
- Side-effect: additional delay on the logic path.

Structured Approach

- Structured DFT approach improves the overall testability with a test-oriented design methodology.
- The most widely used structured design, scan design, attempts to improve testability of a circuit by improving the controllability and observability of storage elements in a sequential design.
- This is done by converting the sequential design into a scan design with three modes of operation: **normal mode**, **shift mode** and **capture mode**.
- In normal mode, all test signals are turned off, and the scan design operates in the functional configuration.

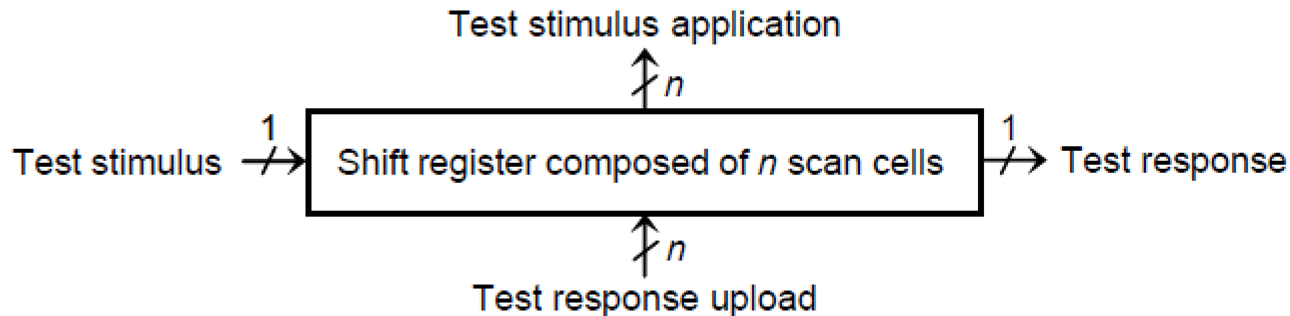
Structured Approach

- In shift and capture mode, TM signal is turned on and all related test procedures are processed.
- Motivation example:

Combinational logic
X_1
X_2
0 → X_3
f
Y_1
Y_2
FF_3
0
Q D
FF_2
1
Q D
FF_1
Q D
CK

Structured Approach

- Scan design simplifies testing difficulty by providing external access to selected storage elements in a design.
- This is done by converting storage elements in **scan cells** and then connecting this scan cells to form shift register, called **scan chain**.



Scan cell design

- Scan cell has two different input sources:
  - **Data input**, driven by the combinational logic,
  - **Scan input**, driven by the output of another scan cell in order to form one or more shift registers, called scan chains.
- These scan chains are made externally accessible by connecting the scan input of the first scan cell in a scan chain to a primary input and the output of the last scan cell in a scan chain to a primary output.
- Because there are two input sources in a scan cell, a selection mechanism should be provided to allow a scan cell to operate in two different modes: *normal/capture mode* and *shift mode*.

Scan cell design

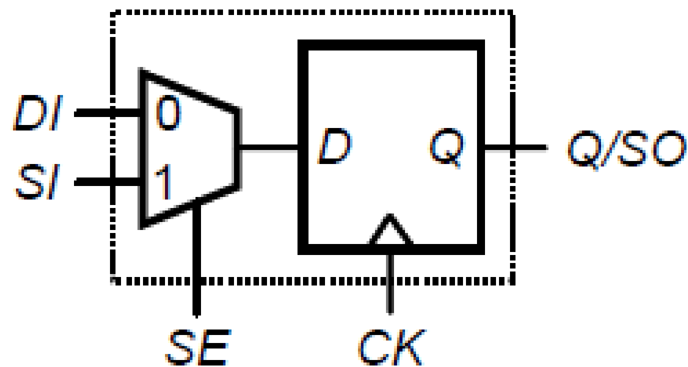
- *normal/capture mode:* data input is selected to update the output.
- *shift mode*: scan input is selected to update the output.

- This makes it possible to shift in an arbitrary test pattern to all scan cells from one or more primary inputs while shifting out the contents of all scan cells through one or more primary outputs.

- We will analyze three common used scan cell designs:
  - Muxed-D scan,
  - Clocked-scan,
  - Level-sensitive scan design.

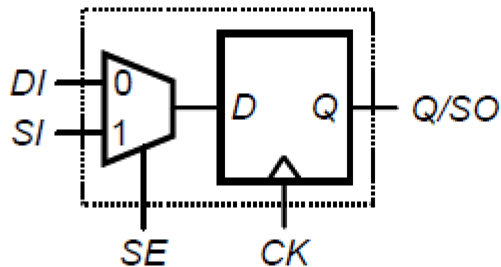
Muxed-D Scan Cell

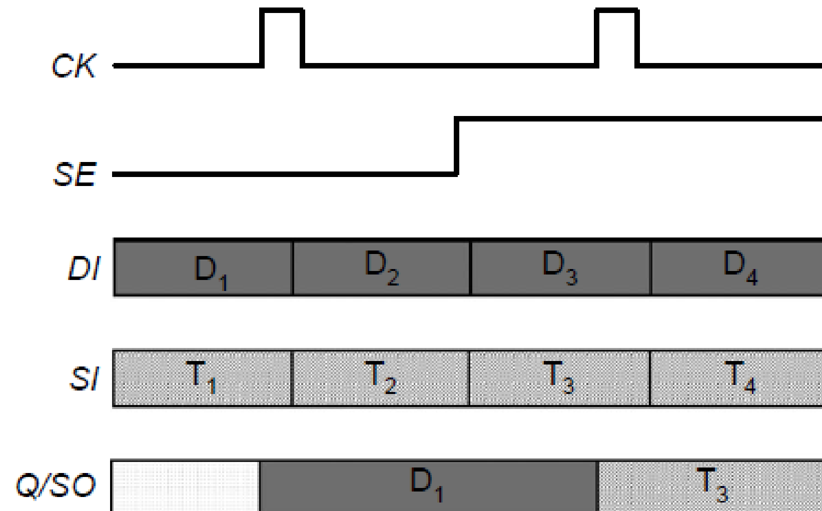
- D storage element is one of the most widely used storage elements in logic designs.
- The most widely used scan cell replacement for the D storage element is the muxed-D scan cell.



Muxed-D Scan Cell

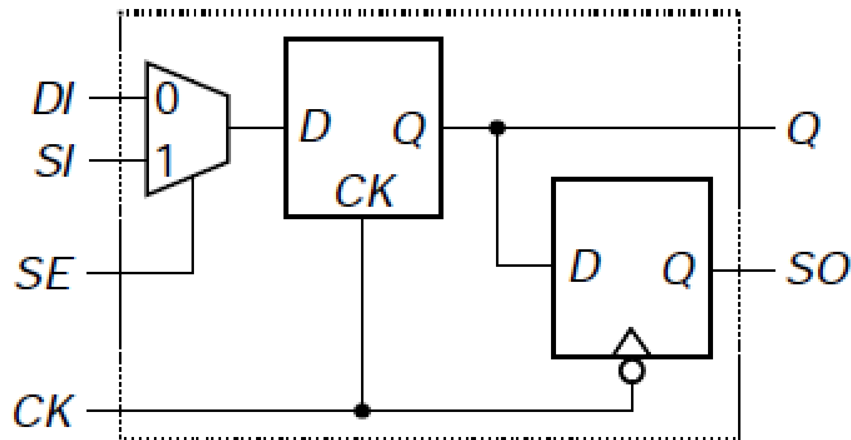
- SE=0
- The value present at the data input DI is captured into the internal D FF when a rising clock edge is applied.
- SE=1
- The value at the SI input is shifted to the D FF while the contents of the D FF is shifted out.





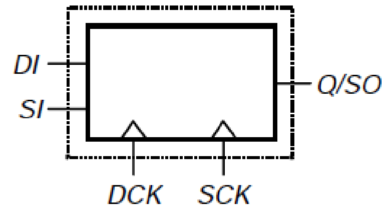
Level-Sensitive/Edge-Triggered muxed-D scan cell

- Composed of a multiplexer, D latch, and D FF.
- Shift operation is edge-triggered.
- Normal and capture operation are level-sensitive.



Clocked-Scan Cell

- Edge-trigggered clocked-scan cell
- Input selection is conducted using two independent clocks, data clock DCK and shift clock SCK.



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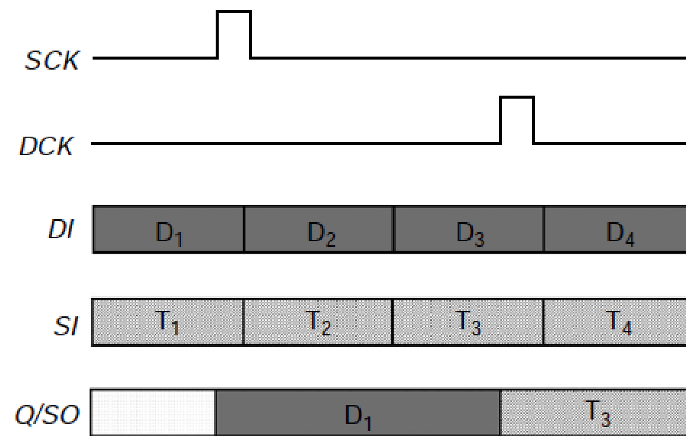

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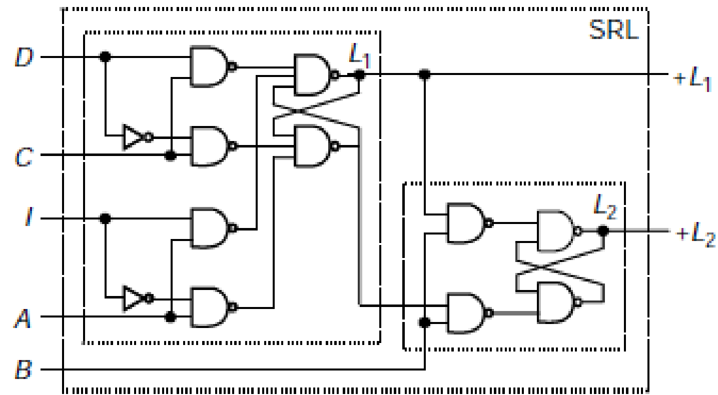
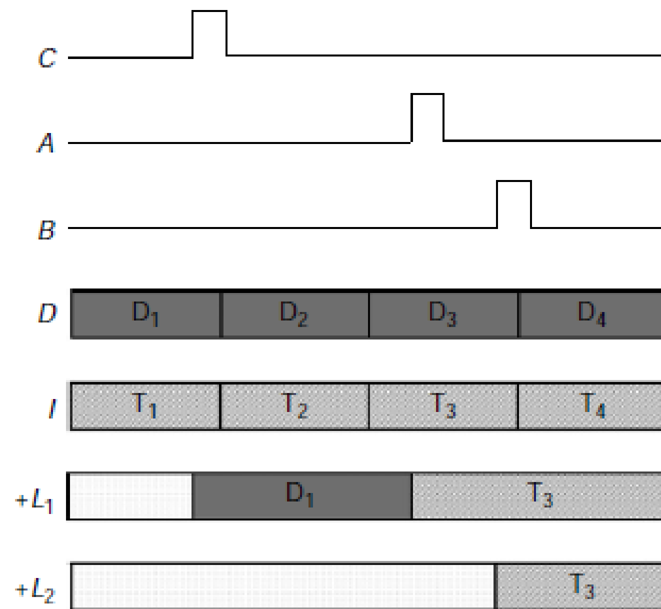
LSSD Scan Cell

- Used for level-sensitive, latch-based designs.
- Scan cell contains two latches:
  - Master two-port D latch L_1
  - Slave D latch L_2
- Clocks *A*, *B* and *C* are used to select between the data input *D* and the scan input *I* to drive $+L_1$ or $+L_2$.
- Normal/capture mode: Clock *C* is used to latch the data *D* onto $+L_1$
- Shift mode: clocks *A* and *B* are used to latch scan data from the scan input *I* and to output this data onto $+L_1$ and then latch the scan data from $+L_1$ onto output $+L_2$ -> used then to drive the scan input of the next scan cell.

LSSD Scan Cell



(a)



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Scan Architectures

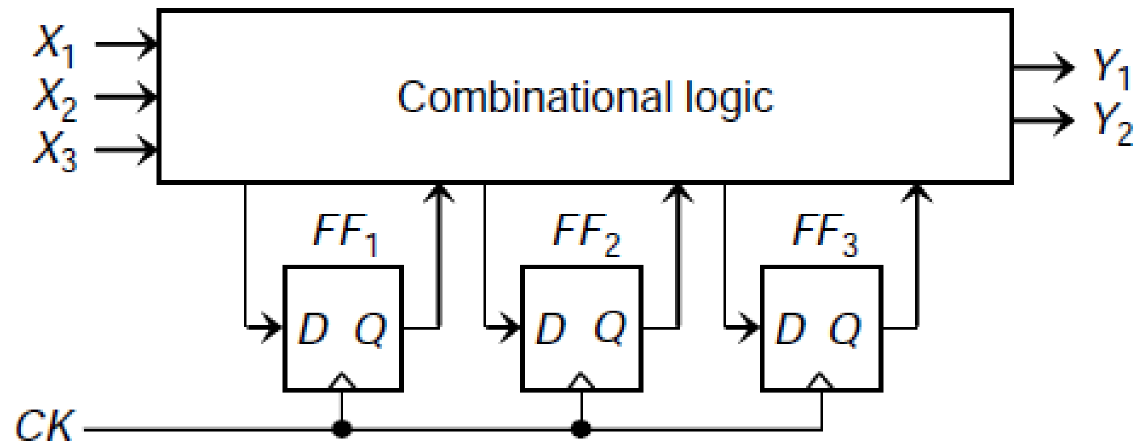
- Full-scan design
  - All storage elements are converted into scan cells and combinational ATPG is used for test generation
- Partial-scan design
  - Subset of storage elements is converted into scan cells and sequential ATPG is typically used for test generation
- Random-access scan design
  - Random addressing mechanism, instead of serial scan chains, is used to provide direct access to read or write any scan cell.

Full-Scan Design

- All storage elements are replaced with scan cells which are then configured as one or more shift registers (scan chains) during the shift operation.
- As a result, all inputs to the combinational logic, including those driven by scan cells, can be controlled, and all outputs from the combinational logic, including those driving scan cells, can be observed.
- Full-scan design converts the difficult problem of sequential ATPG into simpler problem of combinational ATPG.
- Almost full-scan design: a small percentage of storage elements are not replaced for performnce reasons.

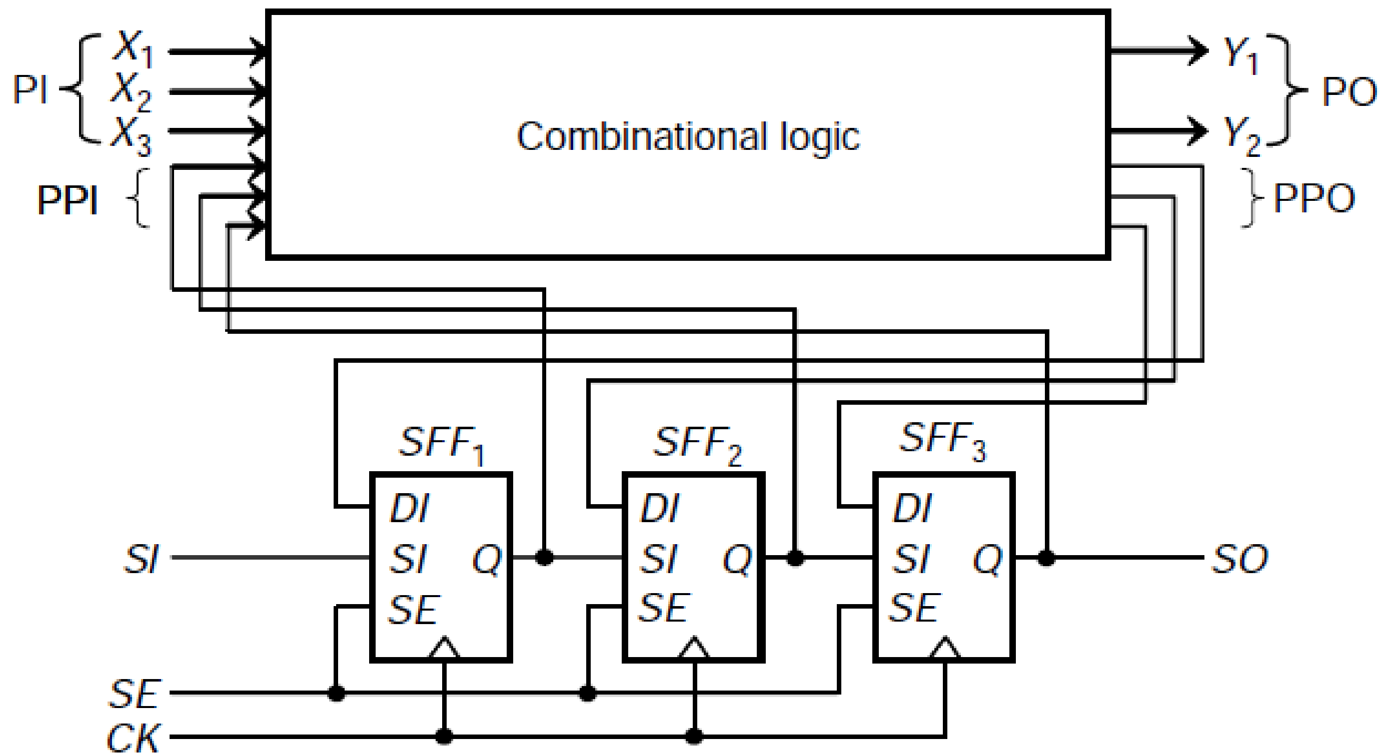
Muxed-D Full-Scan Design

- Example: sequential circuit with three D FF.



Muxed-D Full-Scan Design

- Corresponding muxed-D full-scan circuit.

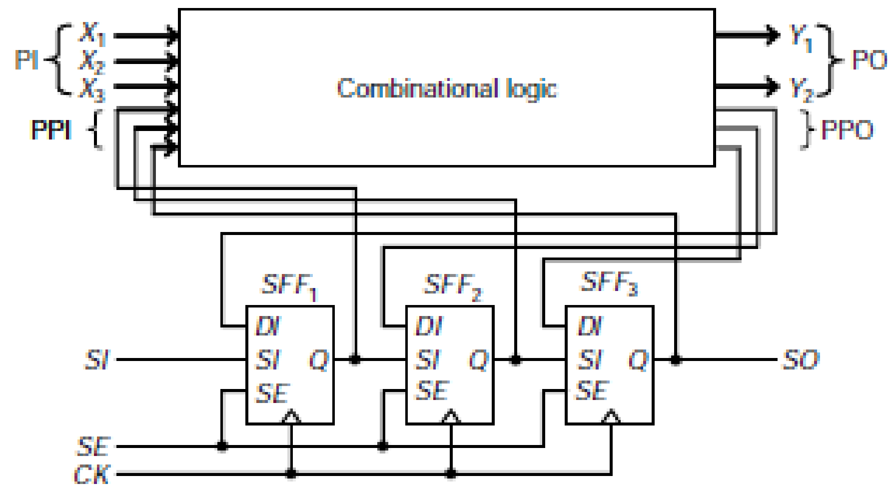


Muxed-D Full-Scan Design

- Shift mode, SE=1: scan cells operate as a single scan chain.
  - Any combination of logic values can be shifted into the scan cells.
- Capture mode, SE=0: scan cells are used to capture the test response from the combinational logic when a clock is applied.

- Primary Input (PI)
- Pseudo Primary Input (PPI): scan cell outputs
- Primary output (PO)
- Pseudo Primary Output (PPO): scan cell inputs

Muxed-D Full-Scan Design



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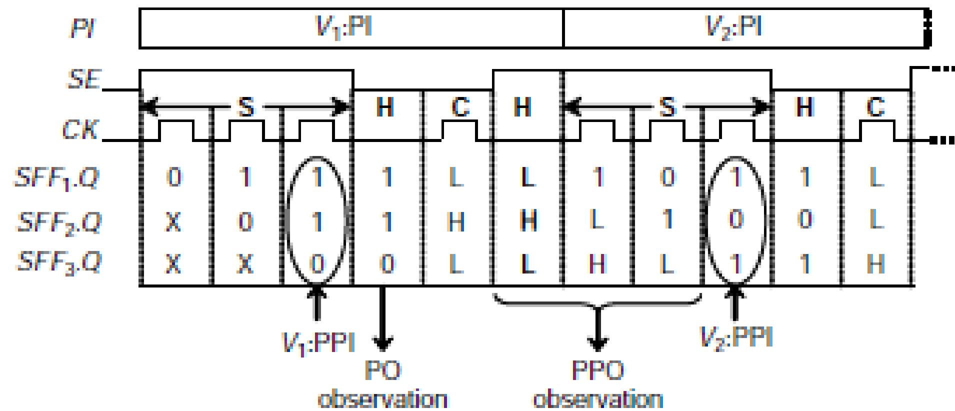
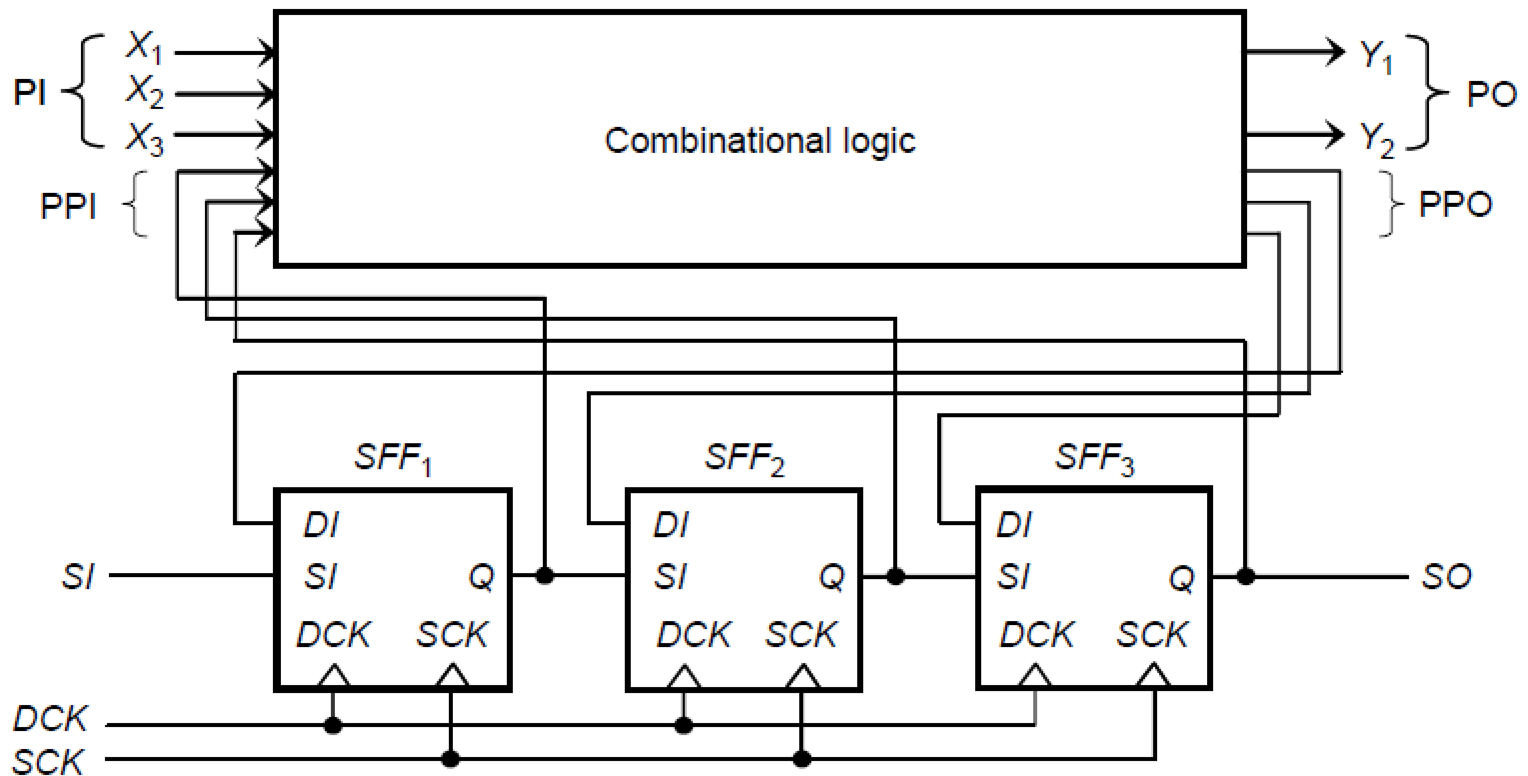


S: shift operation / C: capture operation / H: hold cycle

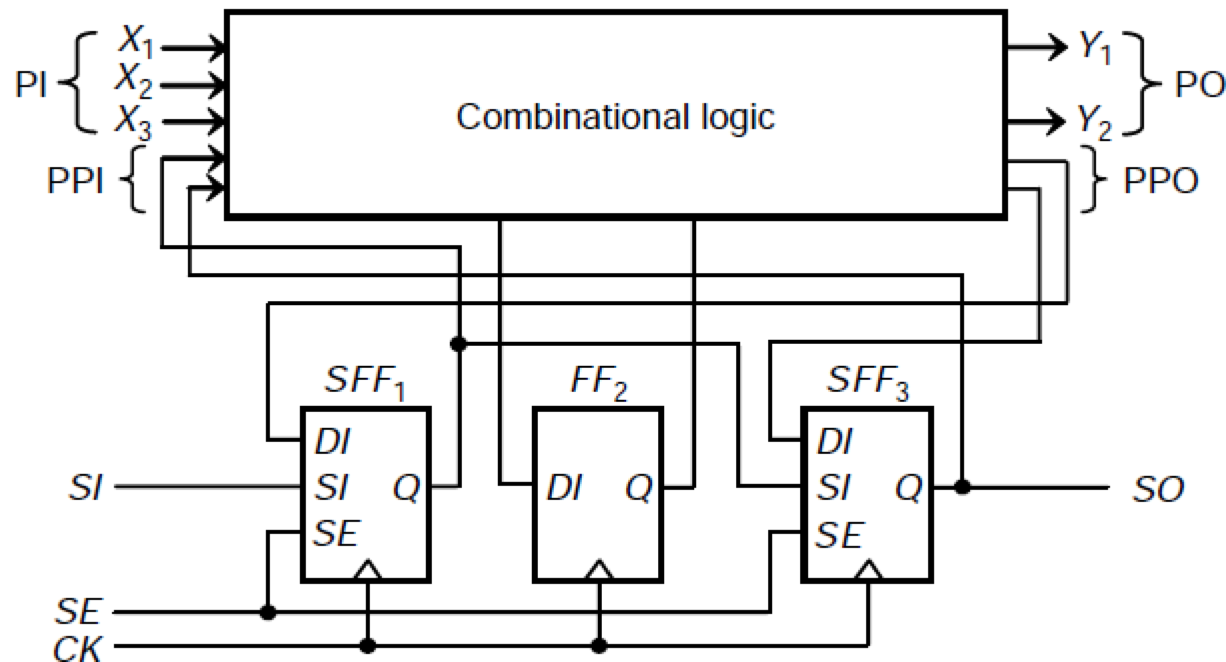
Clocked Full-Scan Design

- Shift and capture mode are distinguished by properly applying 2 independent clocks SCK and DCK.



Partial-Scan Design

- Partial-scan requires only a subset of storage elements to be replaced with scan cells and connected into scan chain
- Example (FF_2 is left out of scan chain):



Scan Design Rules

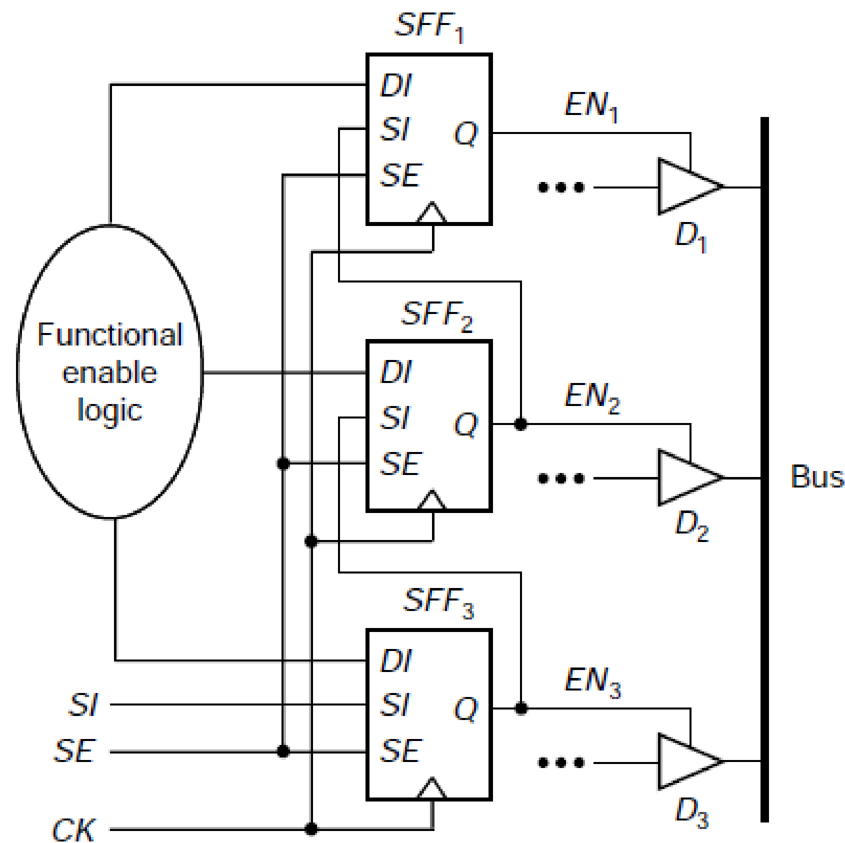
- In order to implement scan into a design, the design must comply with a set of scan design rules.
- Also, a set of design styles should be avoided as they may limit the fault coverage that can be achieved.

Tristate Buses

- Bus contention occurs when two bus drivers force opposite logic values onto a tristate bus, which can damage the chip.
- This does not happen during normal and capture operation.
- But it may happen during shift operation and certain modifications should be made to each tristate bus in order to ensure that only one driver controls the bus.

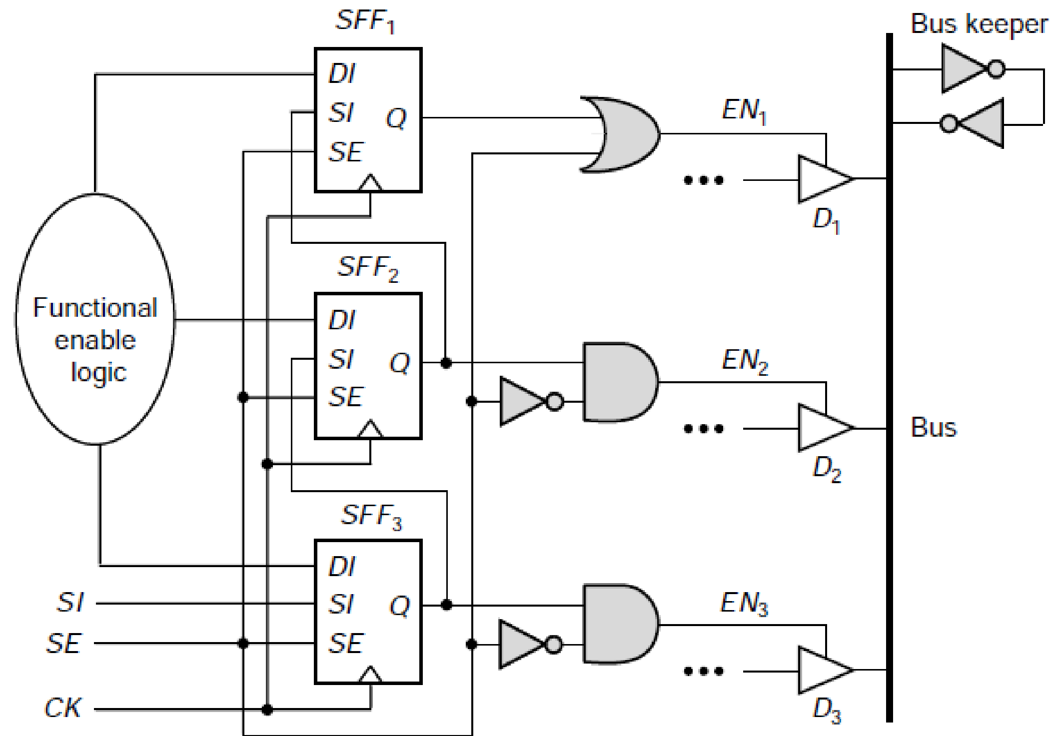
Tristate Buses

- Example, tristaste bus has three bus drivers (D_1, D_2, D_3)



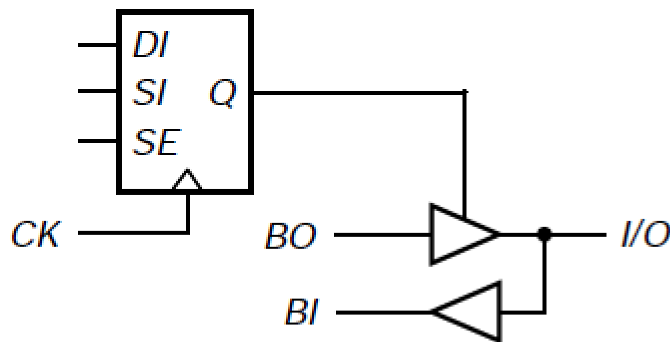
Tristate Buses

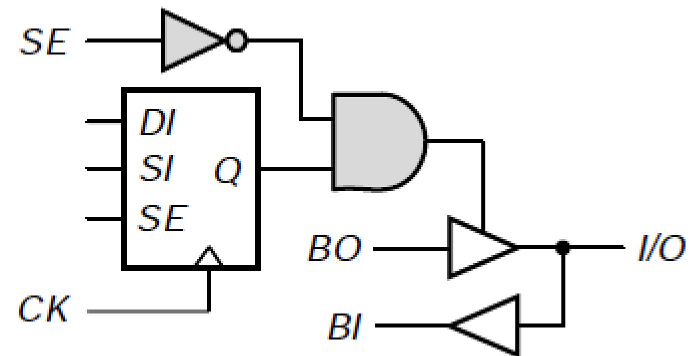
- EN_1 is forced to 1 to enable bus driver D_1, while EN_2 and EN_3 are set to 0 to disable both bus drivers D_2 and D_3, when SE = 1.



Bidirectional I/O Ports

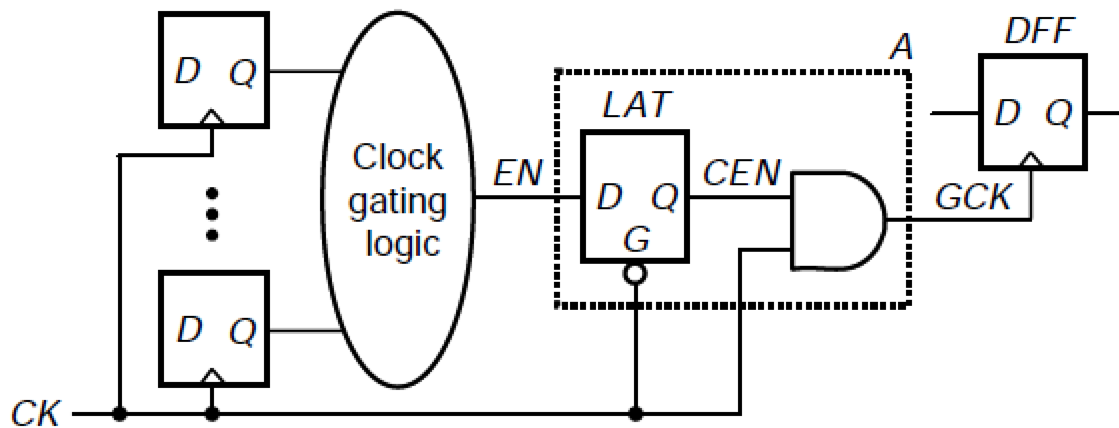
- Used in many designs to increase the data transfer.
- During capture operation, I/O ports are specified as being either input or output -> conflicts may occur during shift operation if the output tristate buffer may become active and the output tristate buffer and the I/O port have opposite logic values.





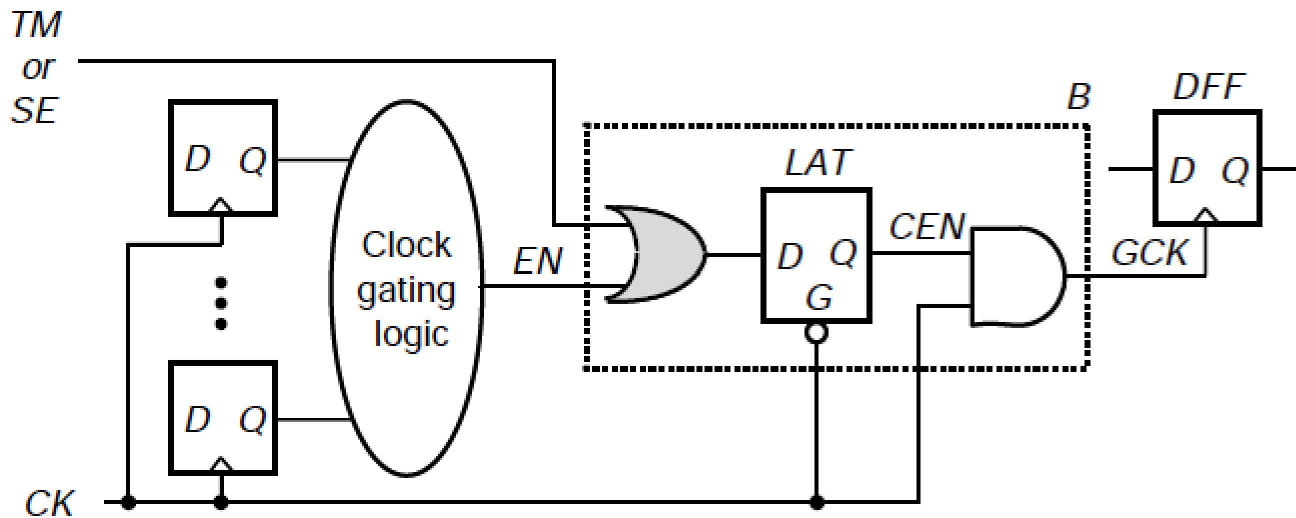
Gated Clocks

- Widely used to reduce power by eliminating unnecessary switching ativity in storage elements.
- Example:



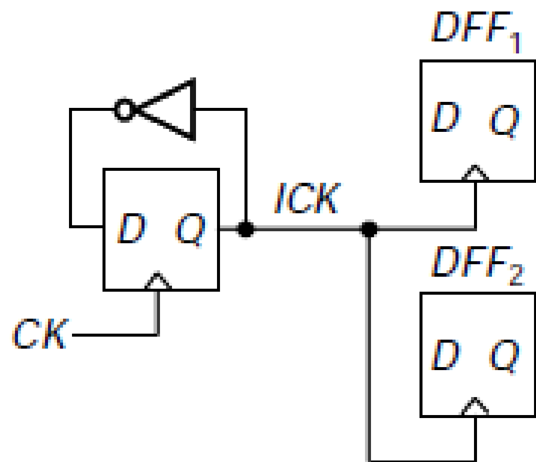
Gated Clocks

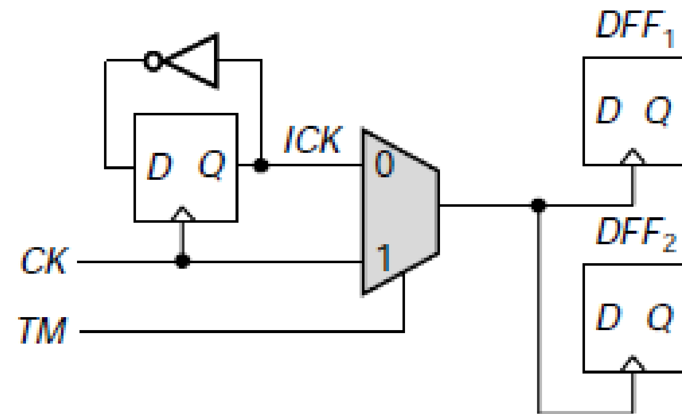
- Modification is required to allow scan shift operation to be conducted on DFF.



Derived Clocks

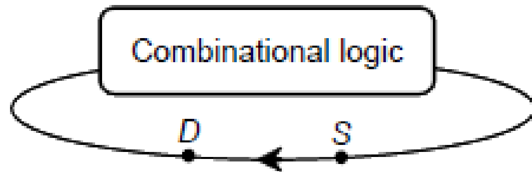
- A derived clock is a clock signal generated internally from a storage element or clock generator.
- Because derived clocks are not directly controllable from PI, these clock signals should be bypassed during testing.

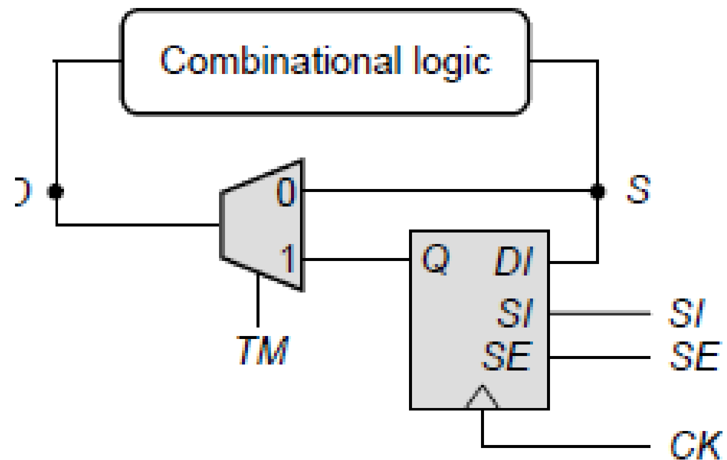




Combinational Feedback Loops

- Loops can introduce either sequential behaviour or oscillation in the design.
- Because the value stored in the loop cannot be controlled or determined during the test, this can lead to an increase in test generation complexity.





Asynchronous Set/Reset Signals

- Asynchronous set/reset signals which are not directly controlled from PI may prevent scan chains from shifting data properly.
- These signals should be forced to an inactive state during the shift operation.