Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

Preizkušanje elektronskih vezij

Uvod

Vsebina predmeta, literatura viri

Izvajalci predmeta

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Izvajanje predmeta

Laboratorijske vaje

Laboratorij za računalniško načrtovanje vezij, LRNV

LAB BN413

Skupina 1:

Ponedeljek, 15:15 - 16:45

Skupina 2:

Torek, 9:15 - 10:45

Literatura

VLSI Test Principles and Applications, Elsevier, 2012, Edited L. Wang, C. Wu, X. Wen

Electronic Design Automation for IC System Design, Verification and Testing, L. Lavagno, I. Markov, G. Martin, L. Scheffer, CRC Press, 2016.

System on Chip Test Architectures, Elsevier, 2012, Edited L. Wang, C. Wu, X. Wen

Vsebina predmeta

- UVOD

Pomen in vloga testiranja, testiranje digitalnih, analognih in mešanih vezij, vpliv tehnologije izdelave vezij VLSI na testiranje.

- TESTNI POSTOPKI ZA VEZJA VLSI IN TESTNA OPREMA

Kako testiramo integrirana vezja? Vrste testiranja. Oprema za avtomatsko testiranje.

- EKONOMIJA TESTIRANJA IN KAKOVOST VEZIJ

Gospodarski vidik testiranja, strošek testiranja, izplen, delež napak, ocena deleža napak.

Vsebina predmeta

- NAČRTOVANJE TESTIRANJA

Metode in pravila za načrtovanja vezij z upoštevanjem testiranja, delni-scan načrt vezja, izvedbe scan-vezij.

- MODELIRANJE NAPAK

Vrste napak, funkcijsko in strukturno testiranje, model enojnih in večkratnih napak, modeliranje stika med povezavami.

- LOGIČNA SIMULACIJA IN SIMULACIJA NAPAK

Modeliranje vezij za logično simulacijo na različnih stopnjah, algoritmi za logično simulacijo, algoritmi za simulacijo napak.

Vsebina predmeta

- AVTOMATSKA GENERACIJA TESTNIH VEKTORJEV

Definicija generacije testnih vektorjev, identifikacija redundantnih napak, sistemi za avtomatsko generacijo testnih vektorjev, testiranje sinhronih in asinhronih vezij.

- TESTIRANJE ZAKASNITEV

Problem testiranja zakasnitev, pristopi k testiranju in ugotavljanju zakasnitev v vezjih.

- TEST IDDQ

Princip testiranja IDDQ in pregled metod, učinkovitost in omejitve testiranja IDDQ.

Vsebina predmeta

- VGRAJENI TESTI

Stroški vgrajenega testa, generiranje testnih vektorjev za vgrajeni test, vstavljanje testnih točk, vgrajeno testiranje pomniških vezij.

- STANDARD ZA OBROBNO TESTIRANJE

Namen standarda, konfiguracija vezja za obrobno testiranje po standardu IEEE 1149.1 (JTAG), vodilo ATP (Analog Test Bus), ciljne napake v analognih vezjih, obrobno testiranje analognih vezij.

Definicija testiranja

- *Testiranje* sistema je eksperiment, pri katerem preverimo delovanje sistema ter ugotovimo ali sistem deluje pravilno.
- V primeru, da delovanje ni pravilno, v postopku *diagnoze* ugotovimo vzrok nepravilnega delovanja.
- Testiranje in diagnoza imata širši pomen.

Pomen testiranja

- Vsako podjetje želi na tržišču ponuditi brezhibne produkte.

- Napake so drage zaradi:
- stroškov odpravljanja napak (ali celo zamenjave izdelkov)
- zmanjšanje ugleda podjetja

- Napake je potrebno čim hitreje odkriti
  - z vsakim kasnejšim korakom se stroški odpravljanje napak povečajo za faktor 10.

Pomen testiranja

- *Rule of Ten*: cost to detect faulty IC increases by an order of magnitude as we move from:
  - device → PCB → system → field operation
    - Testing performed at all of these levels
- Testing also used during
  - Manufacturing to improve yield
    - Failure mode analysis (FMA)
  - Field operation to ensure fault-free system operation
    - Initiate repairs when faults are detected

Nekateri primeri nezadostnega testiranja

- Nekaj najbolj znanih napak:

- Problem prehoda v leto 2000 (millenium bug), napačno obračunavanje datuma in ure
- Izpad električne energije v SV delu ZDA in Kanade (North America Blackout) zaradi napake v programski opremi, ki nadzira elektroenergetsko omrežje
- deljenje s plavajočo vejico pri procesorjih Intel Pentium.

Posledice nezadostnega testiranja

Tudi na drugih področjih:

- Daimler bo po svetu vpoklical več kot milijon avtomobilov zaradi nevarnosti nenamernega sproženja zračnih blazin (17.10.2017).
- Daimlerja, sporočilo: elektrostatična razelektritev v kombinaciji s počeno vzmetjo ure in nezadostno ozemljitvijo elementov krmilnega mehanizma lahko povzroči nenamerno sproženje čelne zračne blazine na voznikovi strani. Popravilo bo vključevalo novo ozemljitev elementov krmilnega mehanizma.
- Audi je v Nemčiji vpoklical 300.000 vozil, saj so v podjetju ugotovili, da se lahko pomožni grelec v modelih A4, A5 in Q5 pregreje in vžge, poroča nemška tiskovna agencija dpa (21. dec. 2017).
- https://svetkapitala.delo.si/keywords/vpoklic-vozil-4742/articles

Posledice nezadostnega testiranja

Tudi na drugih področjih:

Podatki se osvežujejo praktično dnevno (!!)

http://www.zi.gov.si/si/storitve/potrosniki/

- Igrače, igrala, pripomočki, zdravila, mazila, oblačila ….

Posledica slabega testiranja so tudi varnostne luknje:

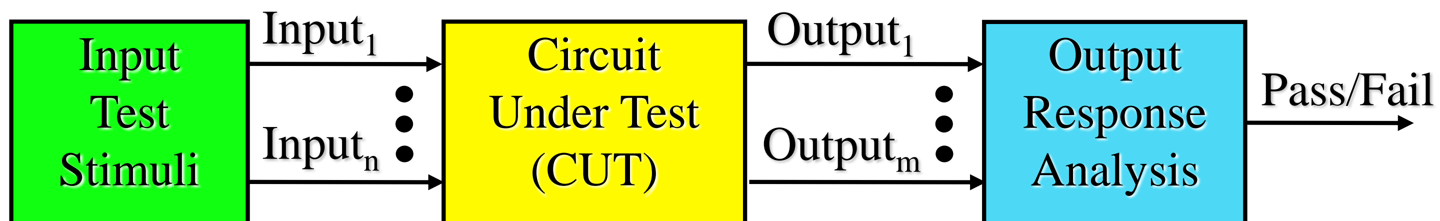
- Nevarna stranska vrata v Intelovi tehnologiji AMT

https://www.racunalniske-novice.com/novice/dogodki-in-obvestila/nova-nevarna-stranska-vrata-v-intelovi-tehnologiji-amt.html

Izvajanje testiranja

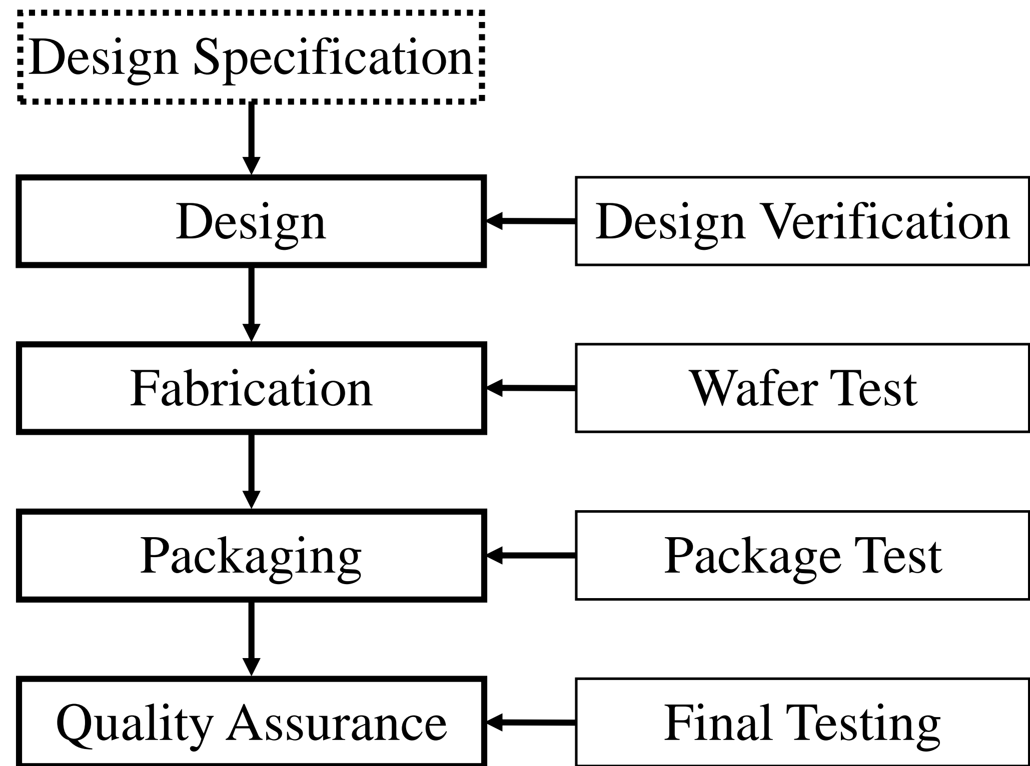
- Testing typically consists of
  - Applying set of test stimuli to inputs of the *circuit under test* (CUT), and
  - Analyzing output responses
    - If correct (pass), CUT assumed to be fault-free
    - If incorrect (fail), CUT assumed to be faulty

Testing is performed at various stages of VLSI development process.



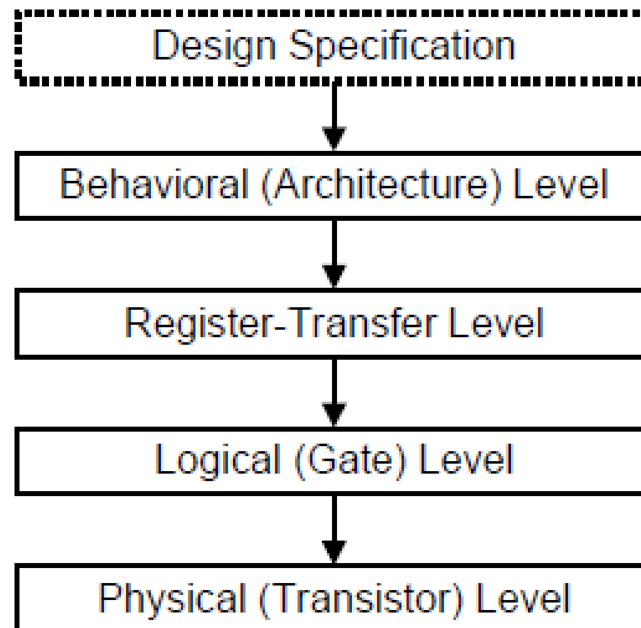
Izvajanje testiranja

- Design verification targets design errors
  - Corrections made prior to fabrication
- Remaining tests target manufacturing defects
  - A defect is a flaw or physical imperfection that can lead to a fault



Izvajanje verifikacije

- Design can be described at different levels of abstraction
  - Design process is a process of transforming a higher level description of a design to a lower level description.



Sinteza, verifikacija, testiranje

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verifikacija

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Testiranje

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.
- Responsible for quality of design.

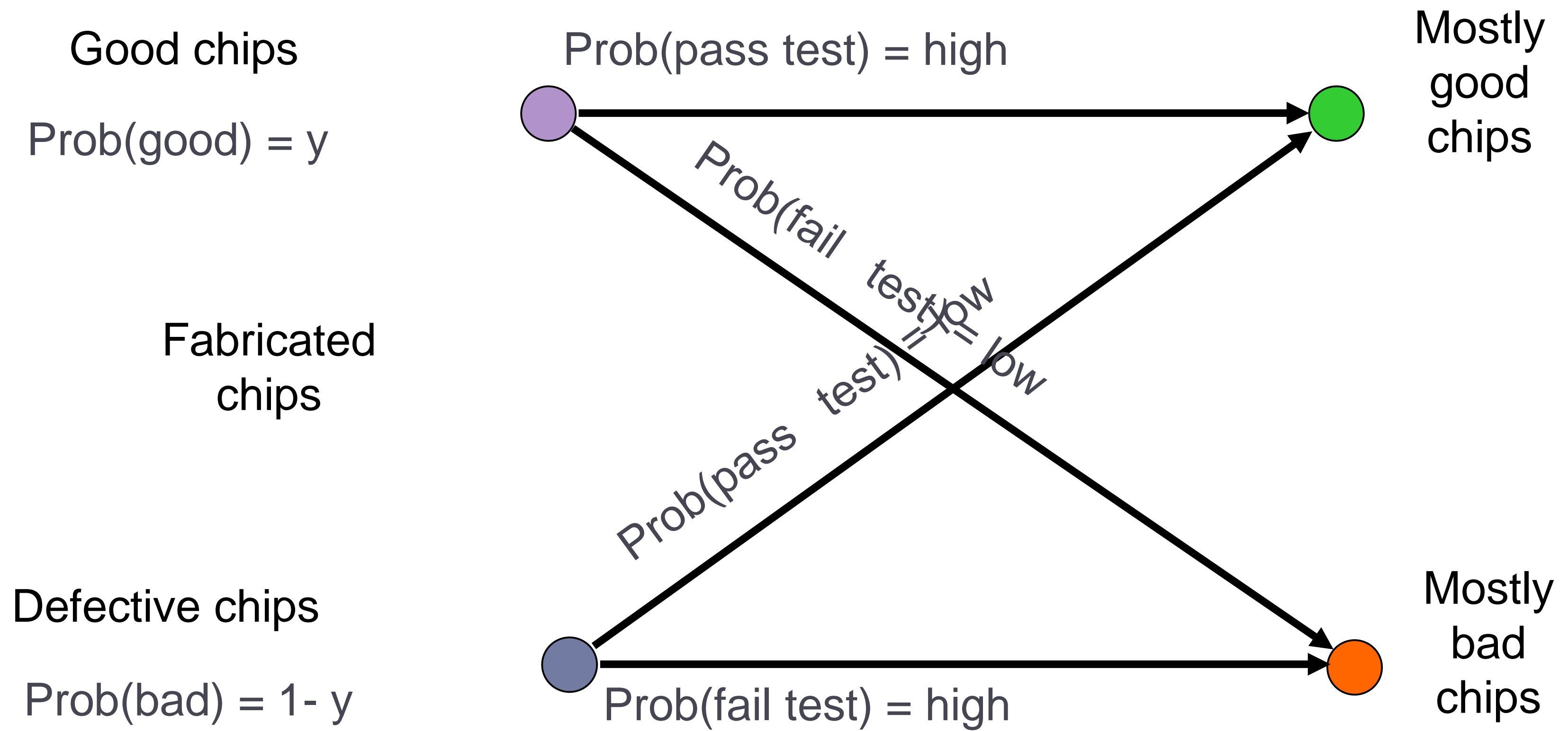
Yield (Izplen)

- The **yield** of a manufacturing process is defined as the percentage of acceptable parts among all parts that are fabricated:

$$Yield = \frac{Number\ of\ acceptable\ parts}{Total\ number\ of\ parts\ fabricated}$$

- Two types of yield loss:
  - 1. Catastrophic (random defects)
  - 2. Parametric (process variations)
- When IC is tested, two undesirable situations may occur:
  - A faulty device appears to be a good part passing the test
  - A good device fails the test and appears as faulty.

Testiranje kot sito



Ideal test

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

Real (realistic) test

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the **yield loss**.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the **defect level**.

Reject Rate (Stopnja zavrnitve)

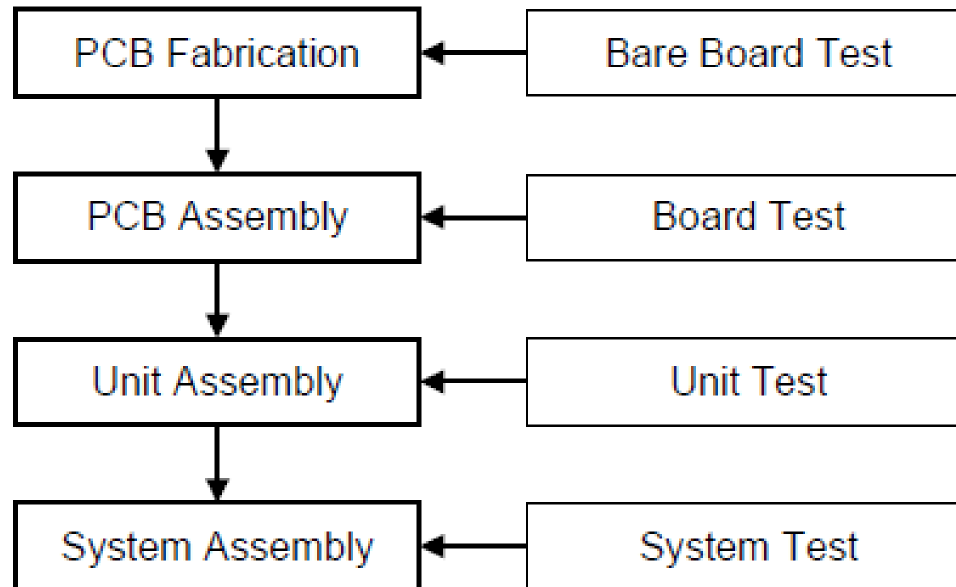
- The ratio of field-rejected parts to all parts passing quality assurance testing is referred to as the **reject rate**, also called the **defect level**.

$$Reject\ rate = \frac{Number\ of\ faulty\ parts\ passing\ final\ test}{Total\ number\ of\ parts\ passing\ final\ test}$$

- Reject rate provides an indication of the overall quality of the VLSI testing process.
- A reject rate of 500 parts per million (PPM) chips may be considered as acceptable, while 100 PM or lower represents high quality.
- The goal of Six Sigma Manufacturing, also referred as zero defect, is 3.4 PPM or less.

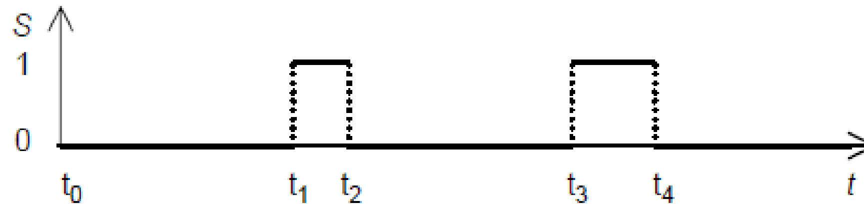
Electronic System Manufacturing Process

- Testing is required at various stages to verify that the final product is fault-free.



System-Level Operation

- State of the system is represented as S, where S=0 means stem operates normally and S=1 represents a system failure.



- Probability that a system will operate normally until time t is referred as realiability:

$$P(T_n > t) = e^{-\lambda t}$$

- λ_i is referred as in individual failure rate

$$\lambda = \sum_{i=0}^{k} \lambda_i$$

System-Level Operation

- The **mean time between failures** (MTBF) is given by:

$$MTBF = \int_0^\infty e^{-\lambda t} dt = \frac{1}{\lambda}$$

- **Repair time** (R) is given by:

$$P(R > t) = e^{-\mu t}$$

- where μ is the repair time and the mean time to repair (MTTR) is given by:

$$MTTR = \frac{1}{\mu}$$

System-Level Operation

- The fraction of time that a system is operating normally (failure-free) is the **system availability**, given by:

$$System\ availability = \frac{MTBF}{MTBF + MTTR}$$

- This equation is used in reliability engineering. Telephone operators are required to have system availability of 0.9999 (four nines).

Vrste testiranja

- Kdaj izvedemo testiranje ?

  - med samim delovanjem (on-line testiranje).

  - kot posebno aktivnost (off-line testiranje).
- Kje je izvor vzbujanja ?

  - v samem vezju (self testing).

  - od zunaj (external testing).
- Kaj testiramo ?

  - napake v načrtu vezja (design verification).

  - napake pri izdelavi vezja (physical faults).

Vrste testiranja

- Kako dobimo testne vzorce ?

  - vnaprej shranjeni v pomnilniku (stored patterned).

  - generirani med samim testiranjem (aut. generated)

- Kako prihajajo vzorci ?

  - vnaprej določenem vrstnem redu.

  - v odvisnosti od predhodno dobljenih rezultatov.

- Kako hitro testiramo vezje ?

  - bistveno počasneje od delovanja vezja (DC testing).

  - s hitrostjo delovanja sistema (AC, at-speed testing).

Vrste testiranja

- Kaj so dobljeni rezultati ?

  - vse izhodne vrednosti.

  - funkcije med posameznimi izhodi (kompaktno test.).

- Katere povezave so dosegljive za testiranje ?

  - samo vhodi in izhodi.

  - vhodi in izhodi ter notranje povezave.

- Kdo preverja izhodne vrednosti ?

  - sam sistem (self-testing).

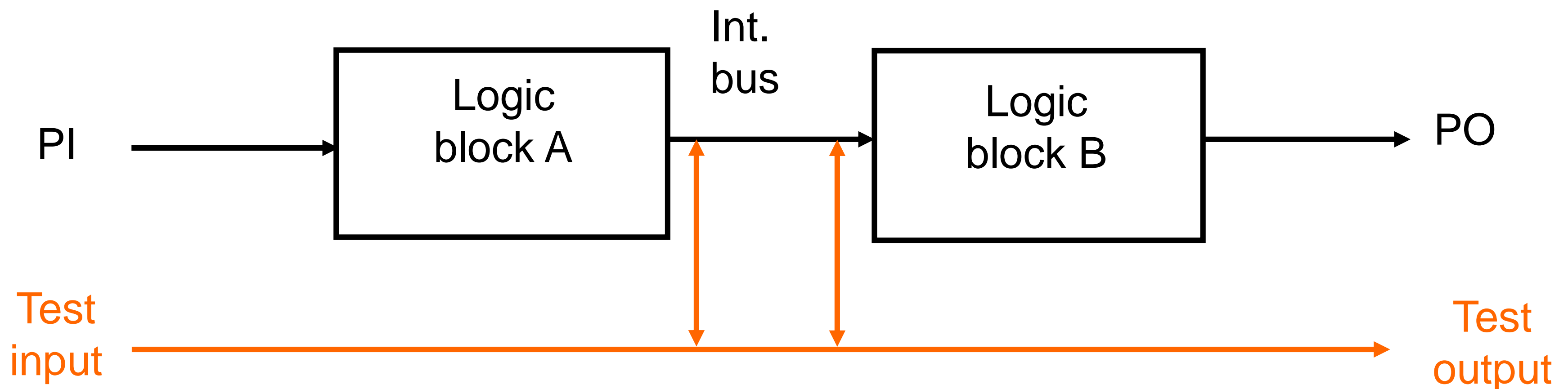
  - zunanja naprava (external testing).

Testing cost

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

Design for Testability

- *DFT refers to hardware design styles or added hardware that reduces test generation complexity*
- Motivation: Test generation complexity increases exponentially with the size of the circuit.
- Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.



Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier.

Types of Manufacturing Tests

- *Wafer sort* or *probe* test – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly sheet resistance, etc.

Sub-types of Manufacturing Tests

- **Parametric**:
  - DC parametric: short test, open test, maximum current test, leakage test, output drive current test, threshold levels.
  - AC parametic test: propagation delay test, setup and hold test, functional speed test, access time test, refresh and pause time test, rise and fall time test.
- These tests are usually technology dependent.
- CMOS voltage output measurements are done with no load while TTL devices require current load.

Sub-types of Manufacturing Tests

- **Functional:**
  - Consists of of the input vectors and the corresponding responses. They check for proper operation of a verified design by testing the internal chip nodes.
  - Functional tests cover a very high percentage of modeled faults (in transistors and wires) in a logic circuits.
  - Often, functional vectors are understood as verification vectors, used to verify whether the hardware actually matches its specification.

Burn-in or Stress Test

- Process:
  - Subject chips to high temperature & over-voltage supply causing bad devices actually to fail.
  - Correlation studies show that the occurance of the potential failures can be accelerated at the elevated temperatures.
- Two types of failures are isolated by burn-in test:
  - *Infant mortality* cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices (caused by a combination of sensitive design and process variation) to actually fail before chips are shipped to customers. Short burn-in (10 – 30 hours, normal environment).
  - *Freak failures* – devices having same failure mechanisms as reliable devices. Long burn-in (100 – 1.000 hours, accelerated environment).

Incoming Inspection

- More comprehensive than production testing
- Tuned to specific systems application
- Often done for a random sample of devices
- Sample size depends on device quality and system reliability requirements
- Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost.

Test Specification and Test Plan

- Device specification document initiates the development activity and contains the following information:
  - **Functional characteristics**: Algorithms to be implemented, I/O signal characteristics (timing waveforms, signal levels) data and control signal behaviour, clock rate.
  - **Type of device**: Logic, microprocessor, memory, analog electronics.
  - **Physical characteristics**: Package, Pin Assignment.
  - **Technology**: CMOS, gate arrays, standard cell, custom
  - **Environmental characterics**: operating temperature range, supply voltage, humidity.
  - **Reliability**: Acceptance quality level (defective parts per million, failure rate per 1.000 hours, noise characteristics).