Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

1. stopnja VSP, 1. letnik

Programirljivi Digitalni Sistemi

Andrej Trost

Literatura: A. Trost: Uvod v programirljive digitalne sisteme, skripta 2016
Spletna stran: http://lniv.fe.uni-lj.si/pds.html

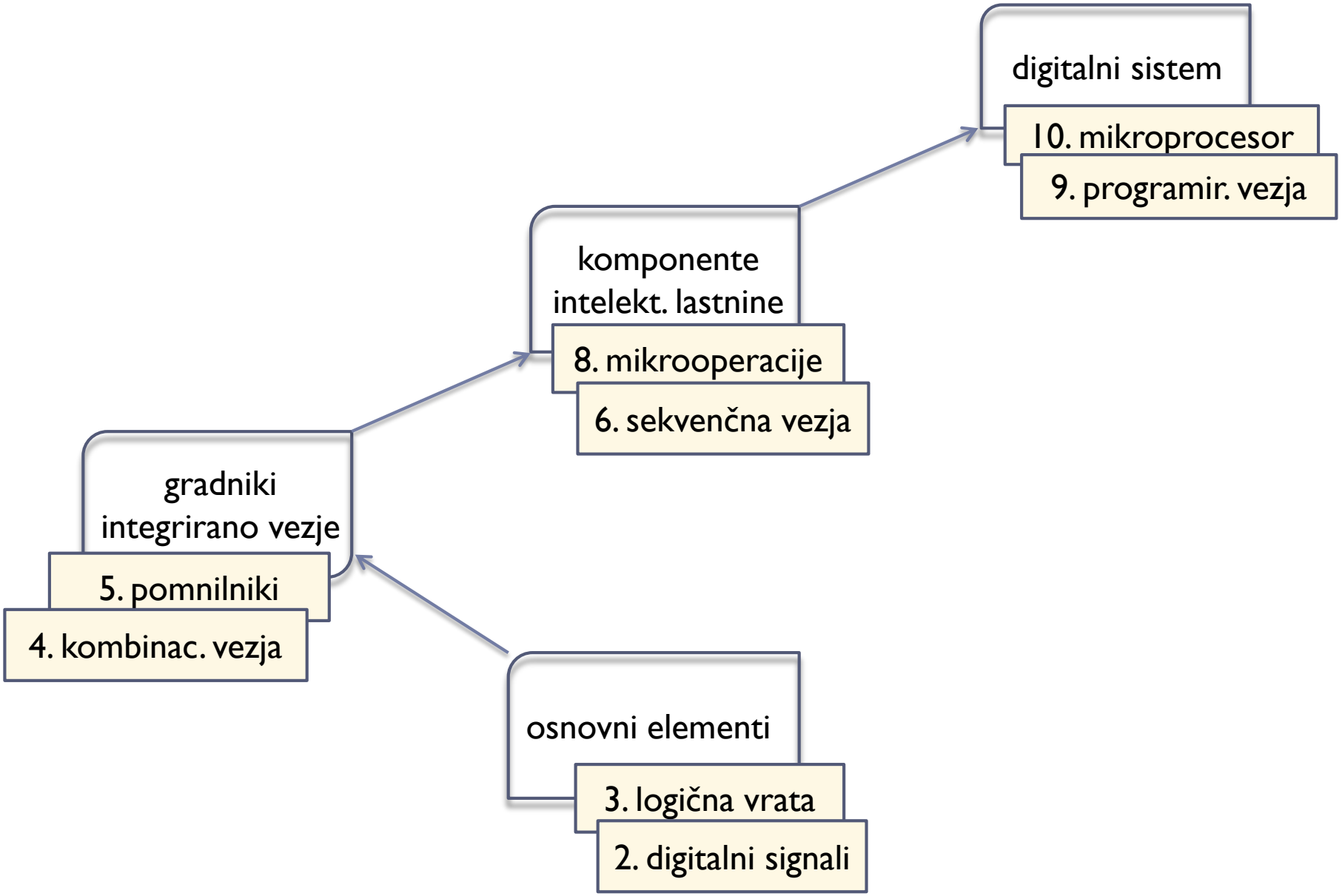
Cilji, izvajanje in ocenjevanje PDS 2017/18

Cilji: študent bo znal

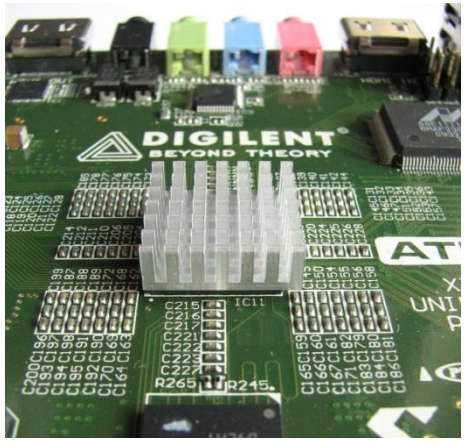
- opisati vrste digitalnih sistemov in njihove gradnike
- uporabiti logične gradnike za reševanje preprostih logičnih nalog
- izdelati shemo logičnega vezja
- razviti opis vezja z diagramom stanj ali mikrooperacijami za dano nalogo
- uporabiti programirljiva vezja
- razlikovati tehnološke izvedbe digitalnih sistemov

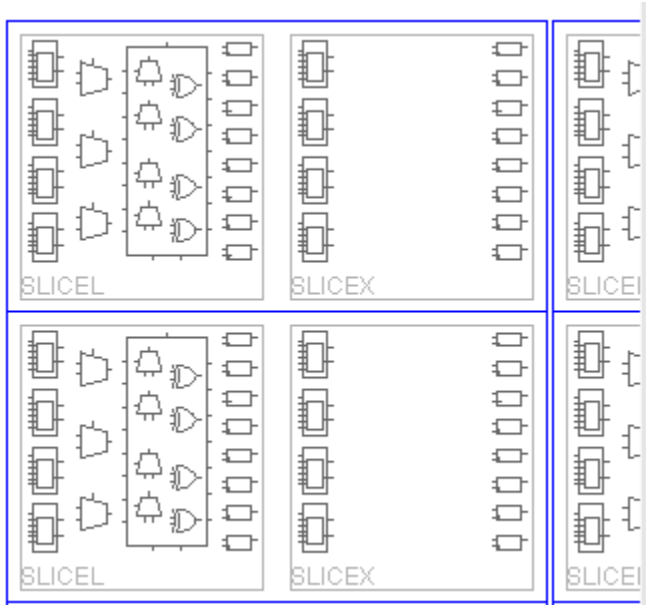
Obveznosti:

- laboratorijske vaje, poročila (pogoj za izpit)
- pisni izpit (obkrožanje) in ustni zagovor

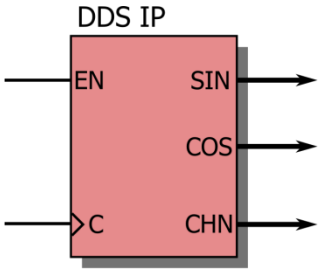

digitalni sistem
10. mikroprocesor
9. programir. vezja
komponente
intelekt. lastnine
8. mikrooperacije
6. sekvenčna vezja
gradniki
integrirano vezje
5. pomnilniki
4. kombinac. vezja
osnovni elementi
3. logična vrata
2. digitalni signali

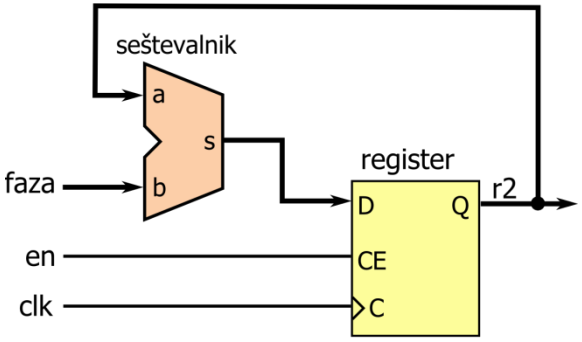
Prototip vezja

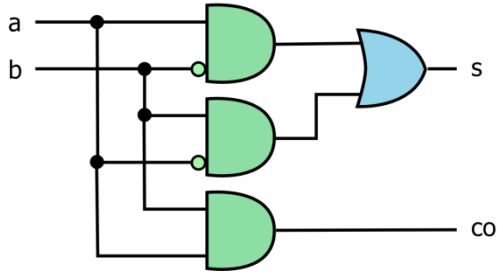




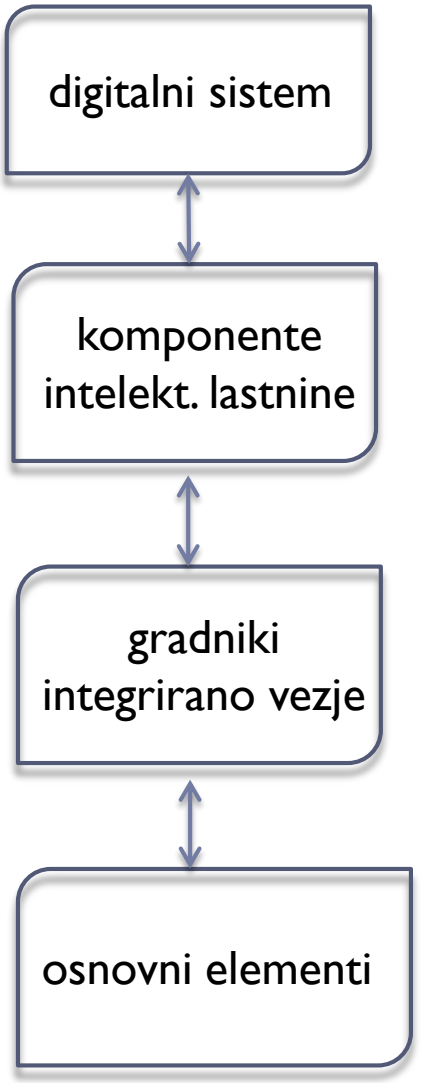
Logični model





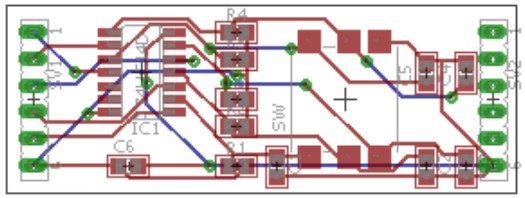


Načrtovanje

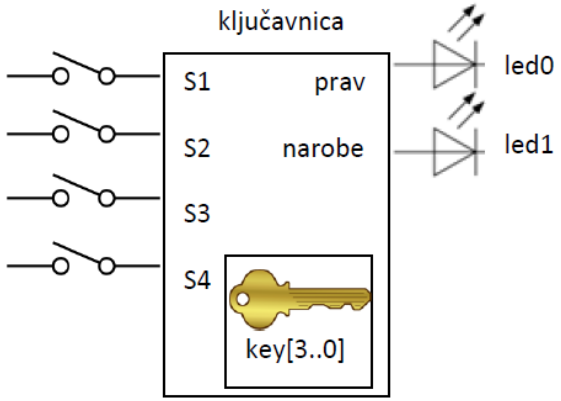


Laboratorijske vaje

- tiskano vezje (Eagle)



- logično vezje, diagram stanj, generator ključev



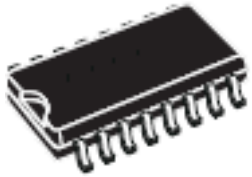
- CPU, slika na monitorju

Razvojni sistem - Altera DE0-Nano

Razumevanje sheme in specifikacij

life.augmented

STP08CP05



SO-16

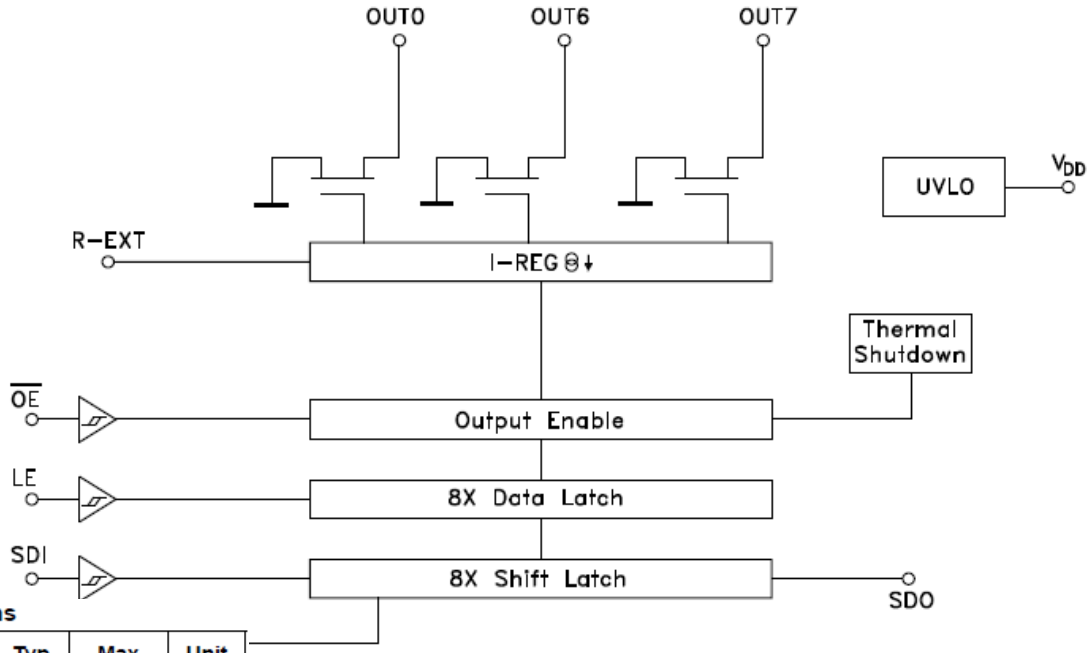
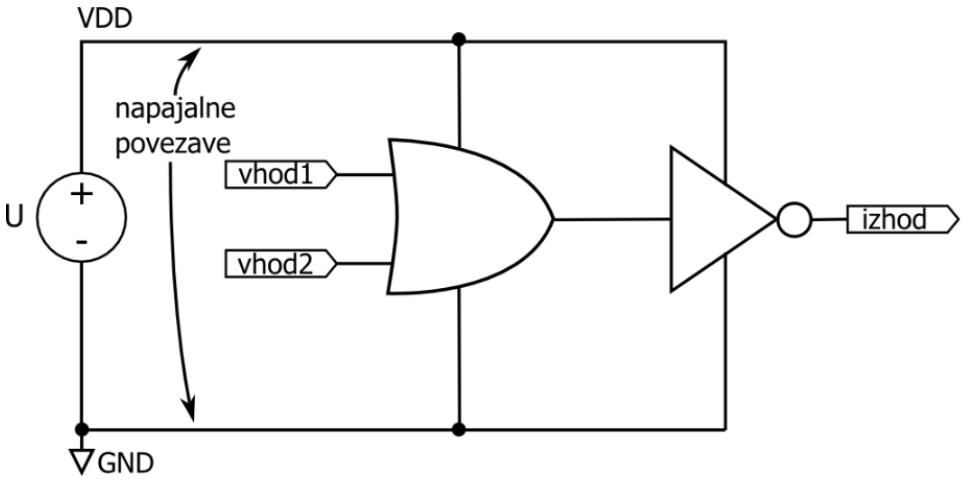
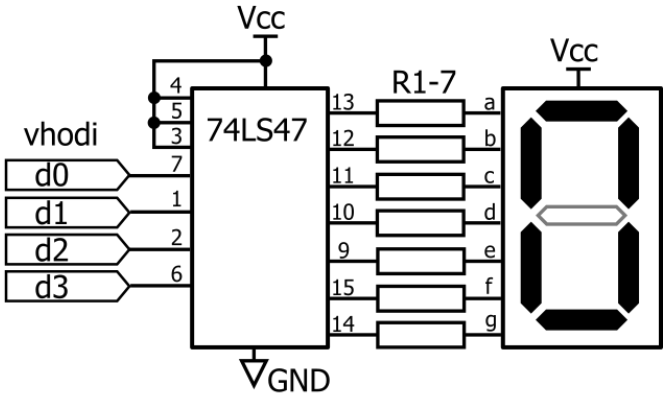


Table 6. Recommended operating conditions

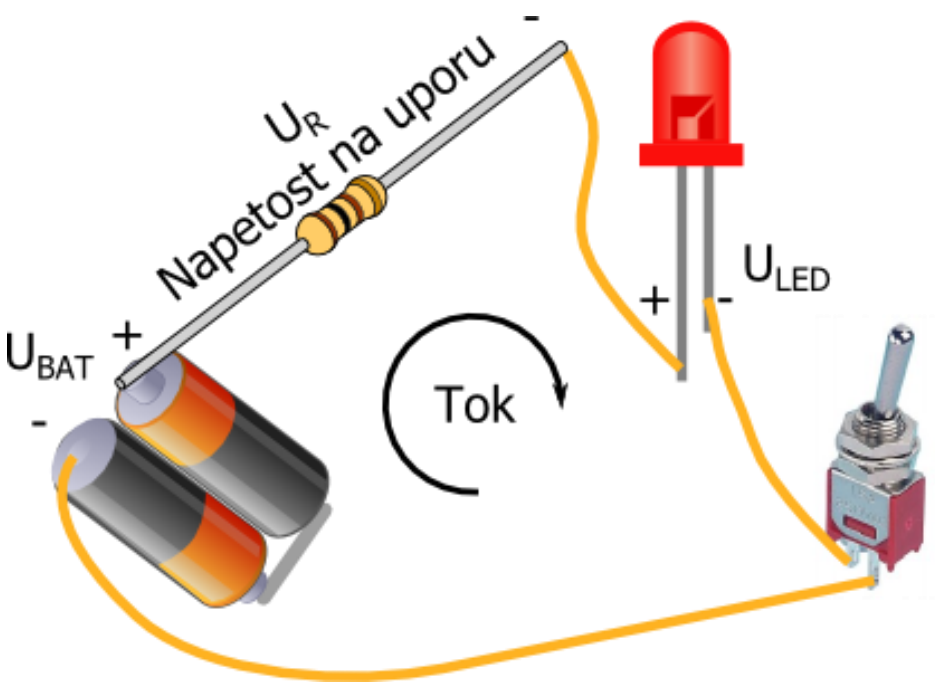
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	5		100	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		0.7 V_{DD}		V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3		0.3 V_{DD}	V
t_{wLAT}	LE pulse width	V_{DD} = 3.0 to 5.0 V	20			ns
t_{wCLK}	CLK pulse width		20			ns
t_{wEN}	$\overline{OE}$ pulse width		200			ns
$t_{SETUP(D)}$	Setup time for DATA		7			ns
$t_{HOLD(D)}$	Hold time for DATA		4			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

Shema digitalnega vezja



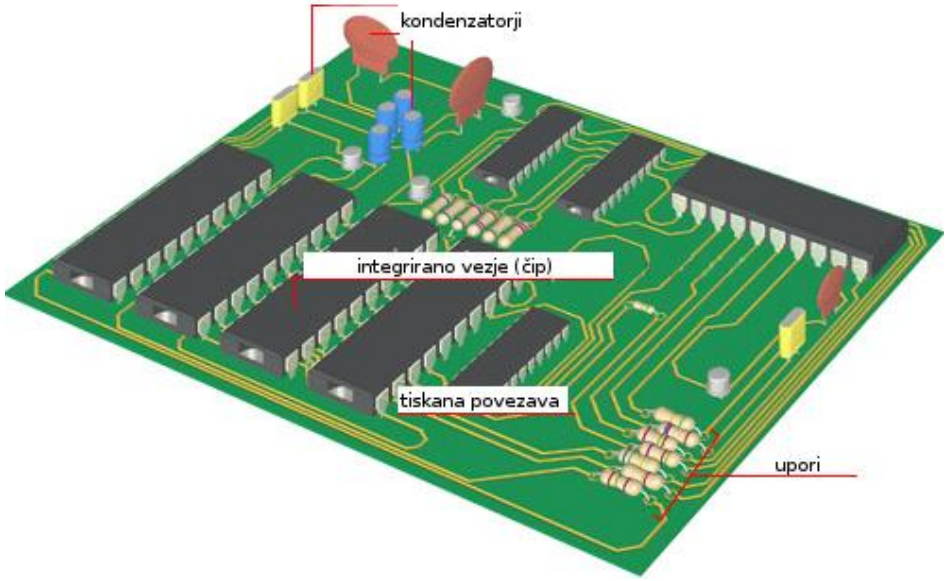


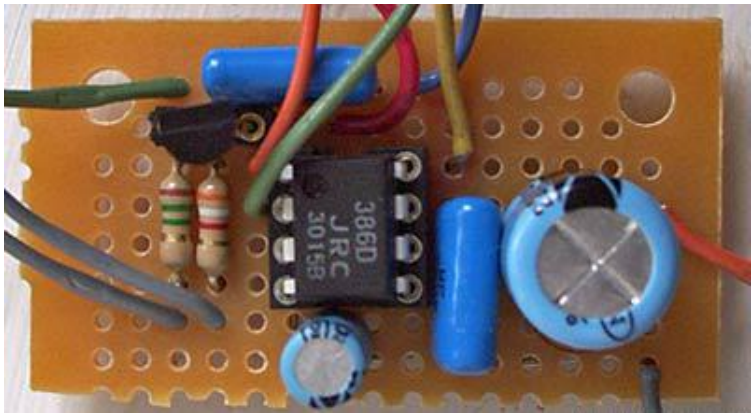
Električno vezje – shema vezja

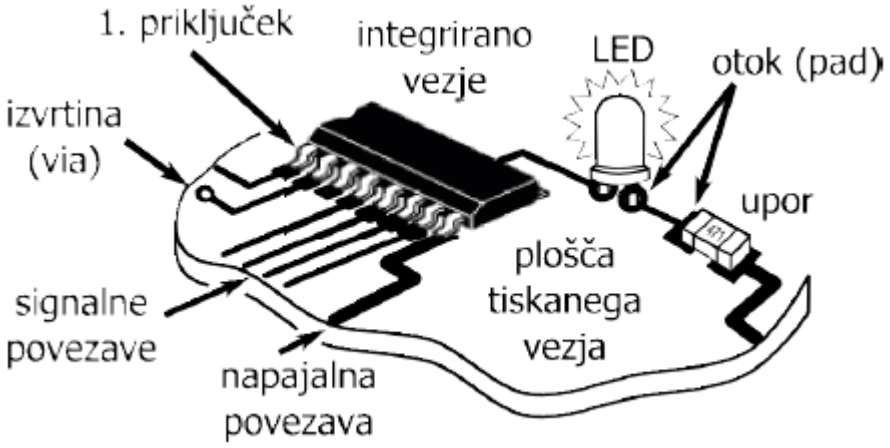


simbol	lastnost	element
R ali R	upornost [Ω]	upor
C ali C	kapacitivnost [F]	kondenzator
+ U - ali + U -	napetost [V]	baterija ali vir napetosti
	preklopi tokokrog	preklopno stikalo
	sklene tokokrog	tipka
	sveti ko teče tok v smeri ▷|	svetleča dioda (angl. LED)
ali	vhodni signal	
ali	izhodni signal	
Vdd ali Vcc	napajalni nivo	
GND ali GND	masa	

Tiskano vezje



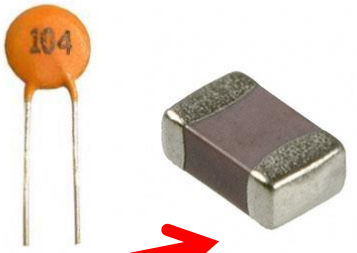




Komponente elektronskega vezja

upori

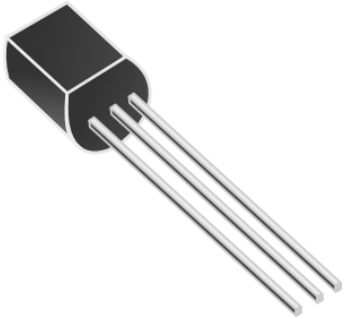
kondenzatorji

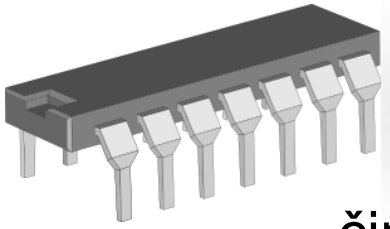


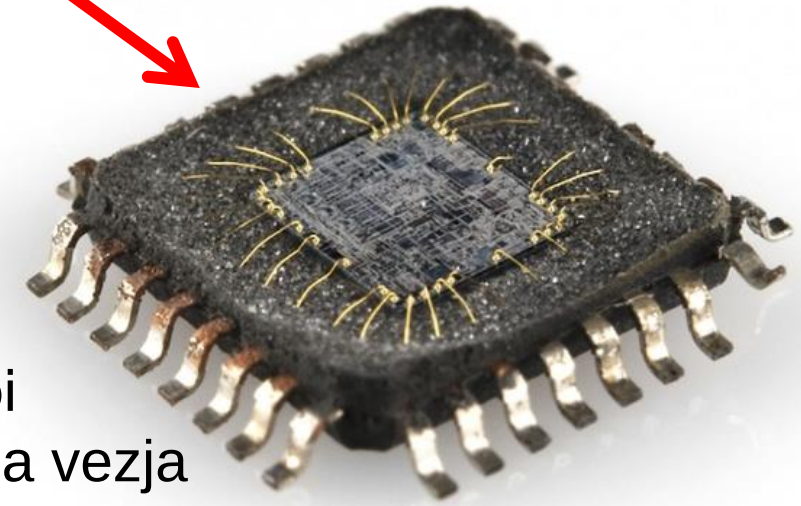
površinska montaža

SMD

tranzistorji





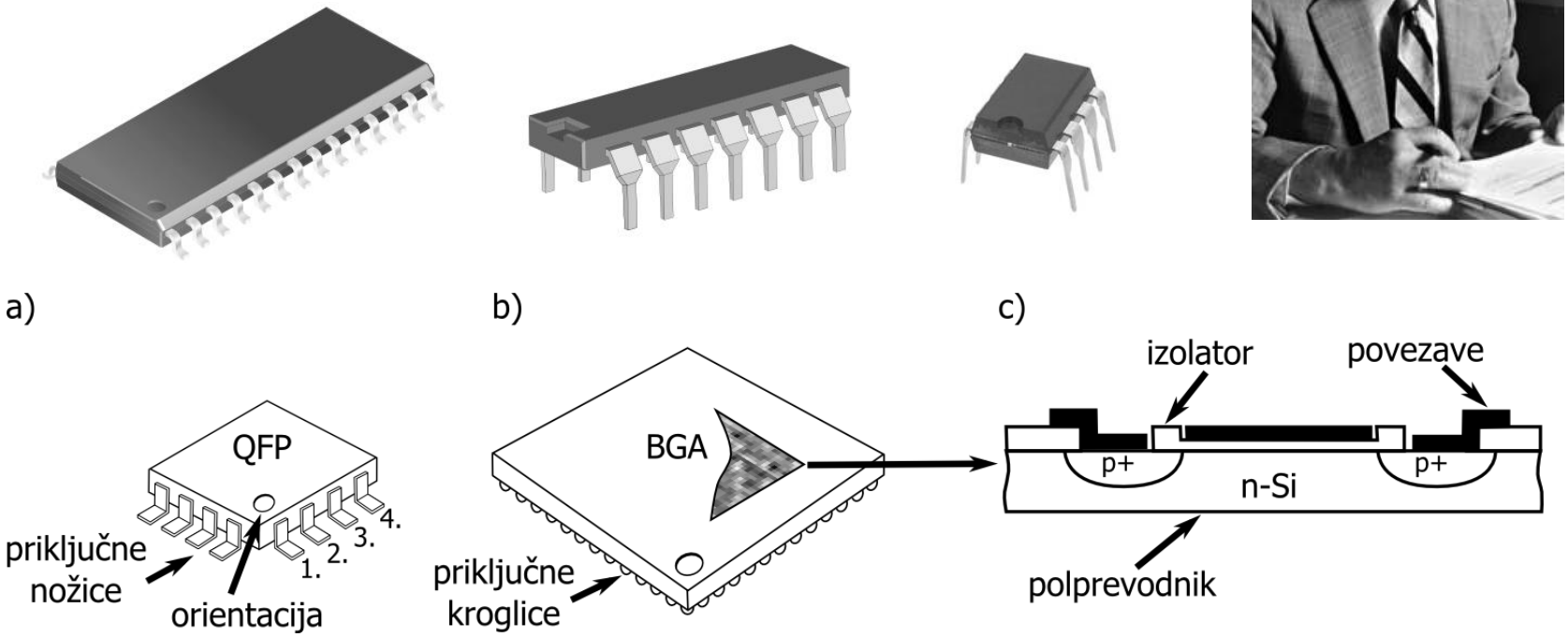


čipi

integrirana vezja

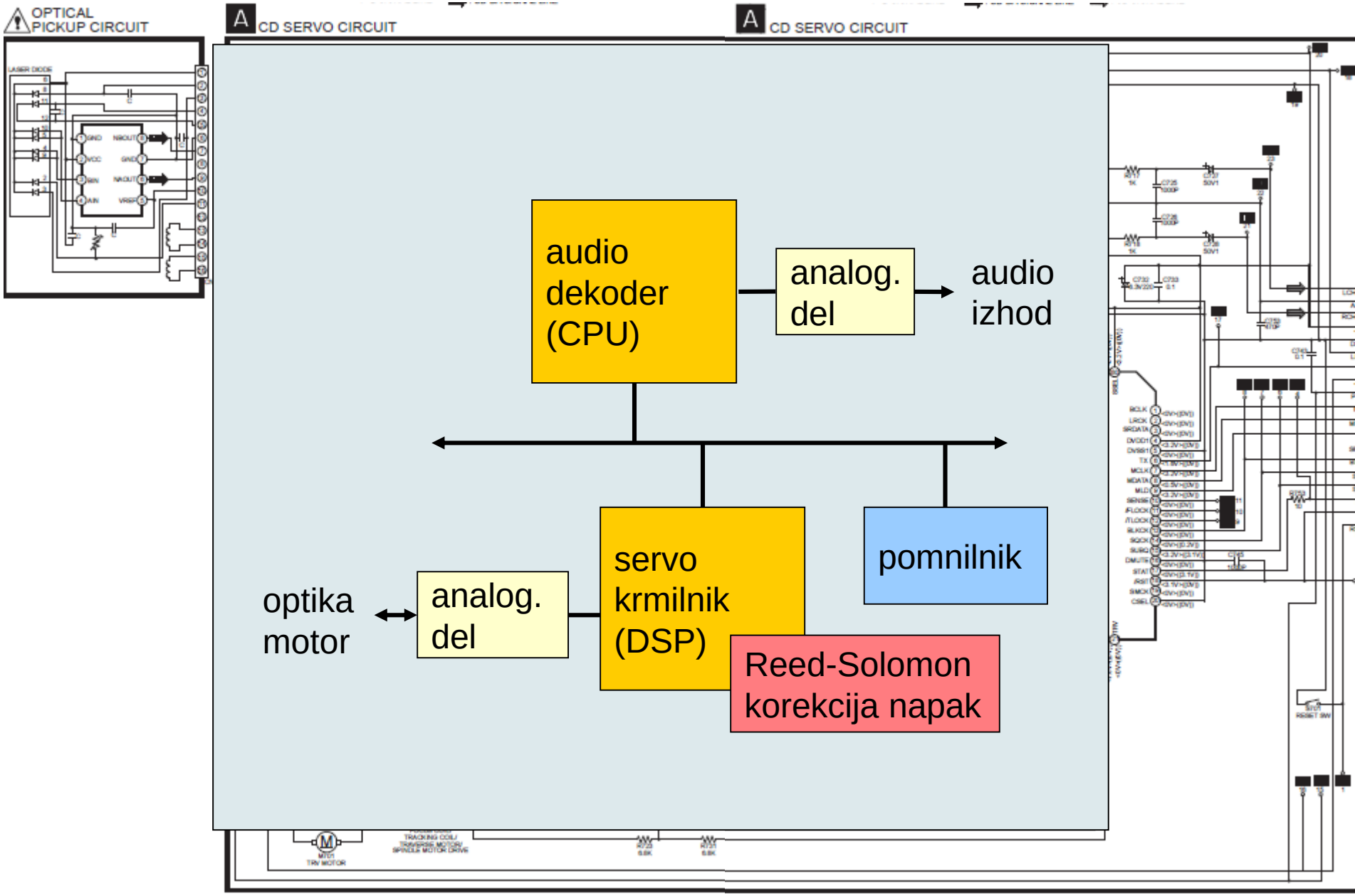
Integrirana vezja

- J. Kilby in R. Noyce izumila mikroelektronsko vezje na rezini polprevodnika – integrirano vezje

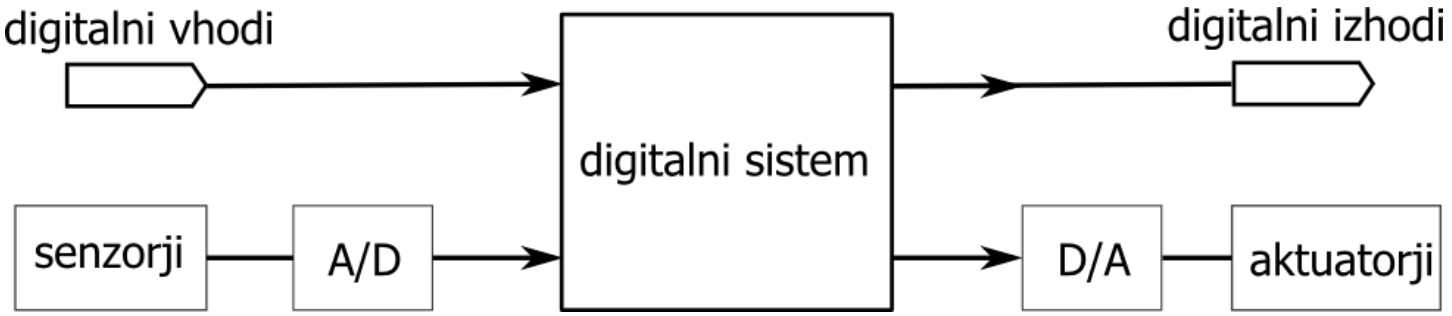


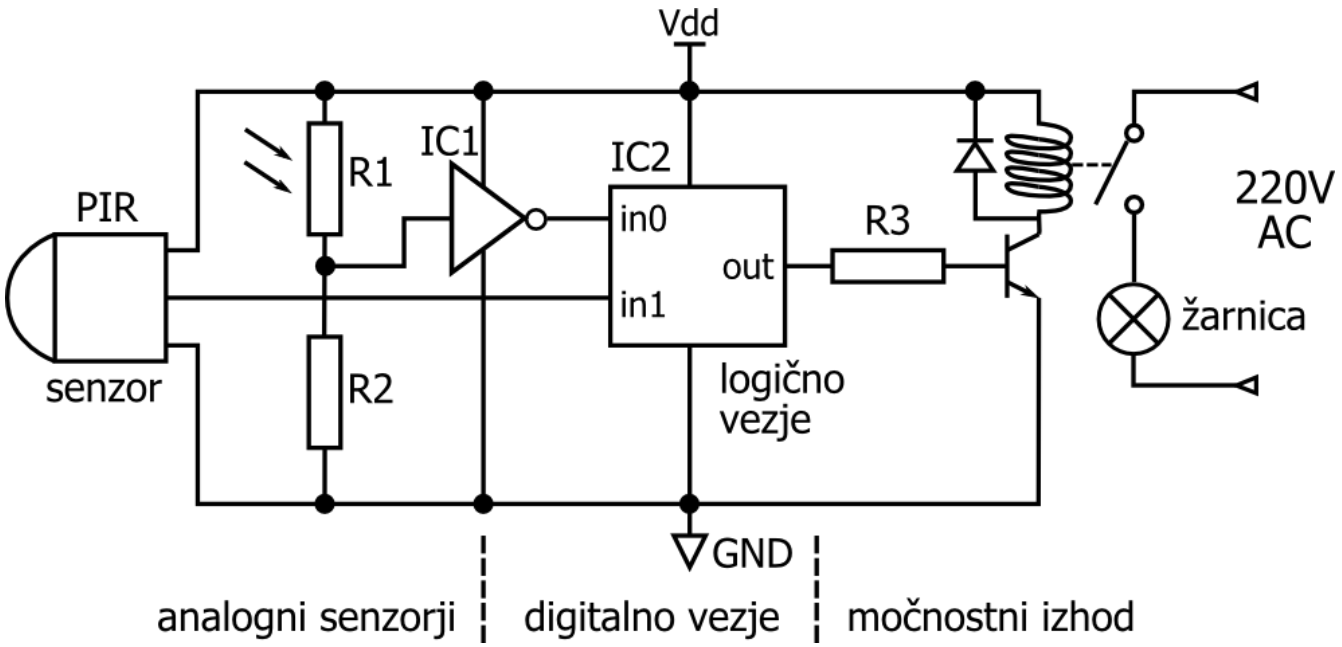
Sodobno integrirano vezje v ohišju QFP (a) in BGA (b), prerez silicijeve rezine z vezjem (c)

Motivacija


OPTICAL PICKUP CIRCUIT
A CD SERVO CIRCUIT
A CD SERVO CIRCUIT
audio dekoder (CPU)
analog. del
audio izhod
servo krmilnik (DSP)
pomnilnik
optika motor
analog. del
Reed-Solomon korekcija napak

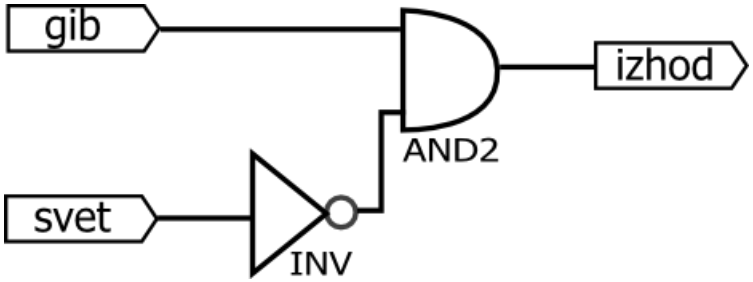
Digitalni sistem

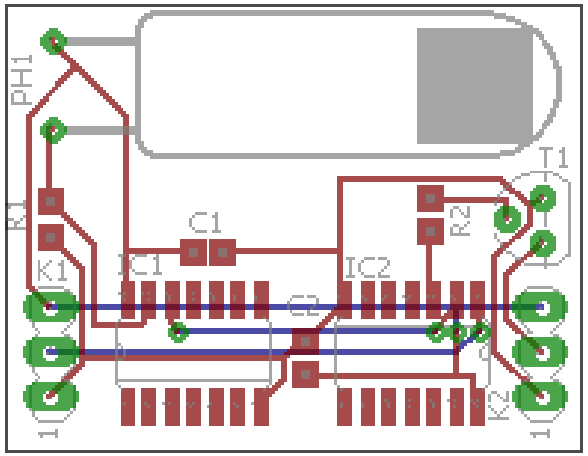




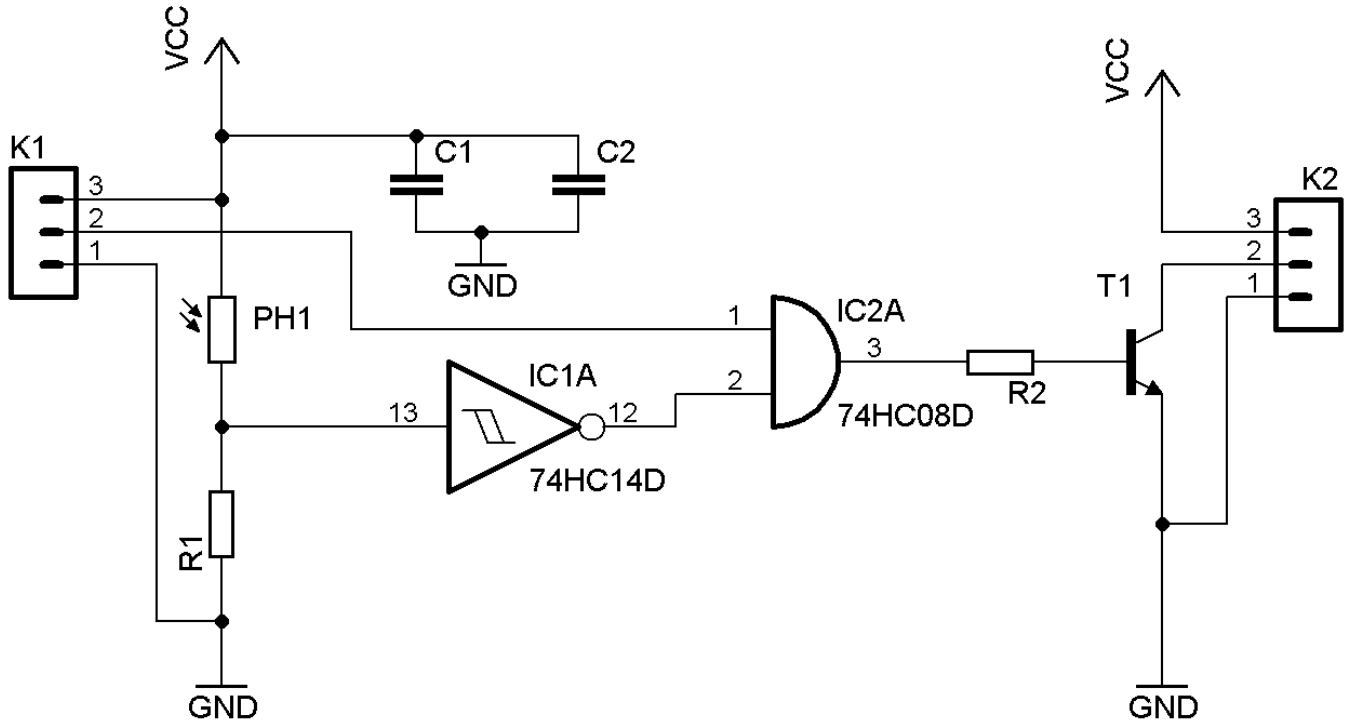
Izvedba sistema

- logična shema



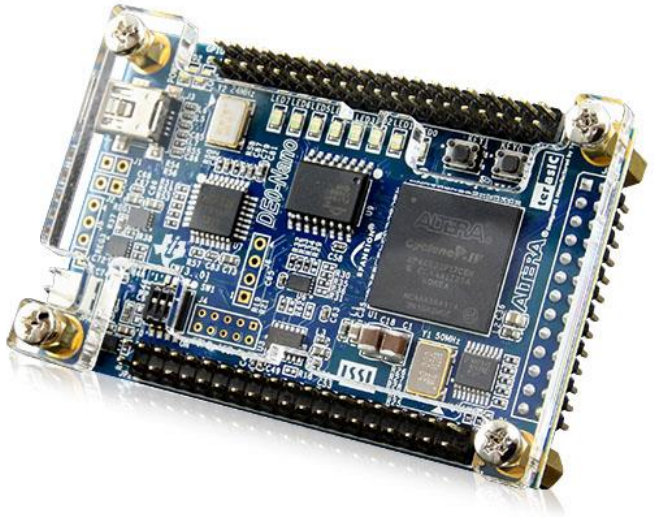


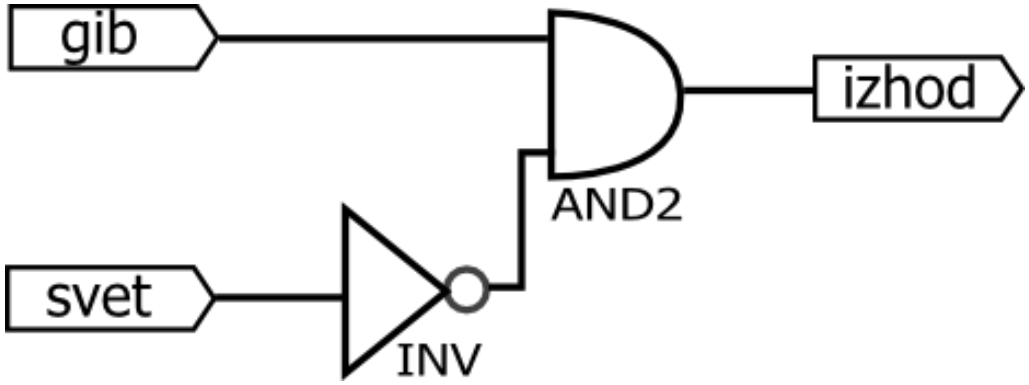
- shema tiskanega vezja



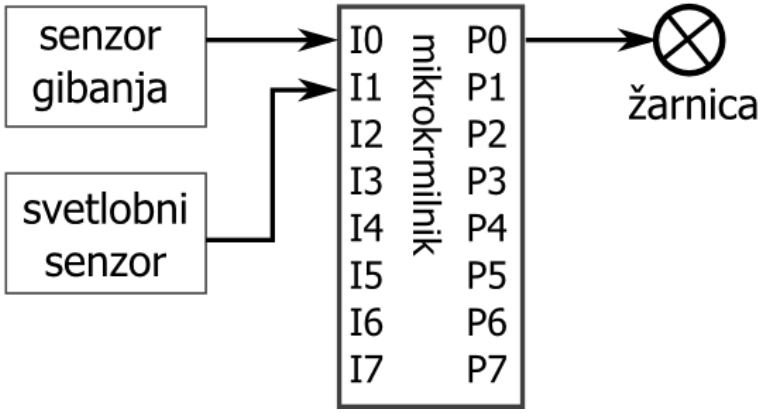
Računalniški opis

```
1   entity senz is
2      port ( gib   : in    std_logic;
3             svet  : in    std_logic;
4             izhod : out   std_logic);
5   end senz;
6
7   architecture opis of senz is
8   begin
9    izhod <= gib and (not svet);
10  end opis;
```





Mikroprocesor – mikrokrmilnik




```
1   while (1) {
2       gib = digitalRead(in0);
3       svet = digitalRead(in1);
4
5       if (gib & svet) digitalWrite(out, 1);
6       else digitalWrite(out, 0);
7   }
```