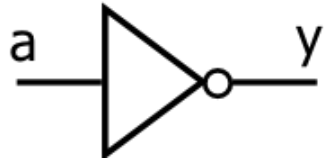
Boolova logična vrata

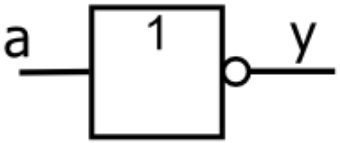
- Logične funkcije nad binarnimi vrednostmi: 0 in 1
- Najbolj preprost gradnik je negator
  - en vhodni in en izhodni signal
  - izhod ima invertirano (negirano) vrednost glede na vhod

y = NOT (a)

značilen simbol:

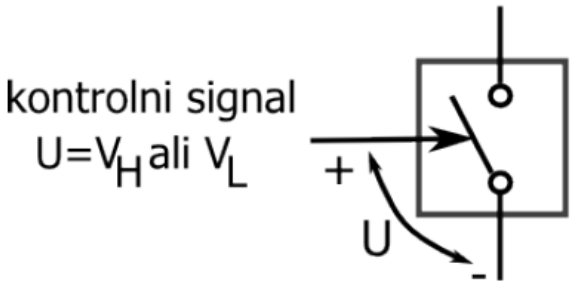


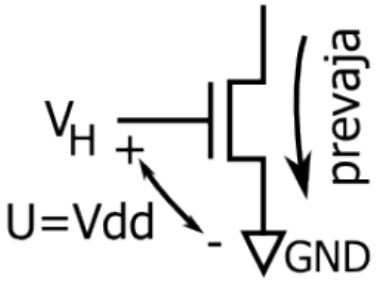
IEEE simbol:

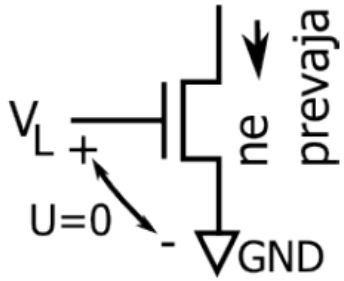


Elektronska stikala

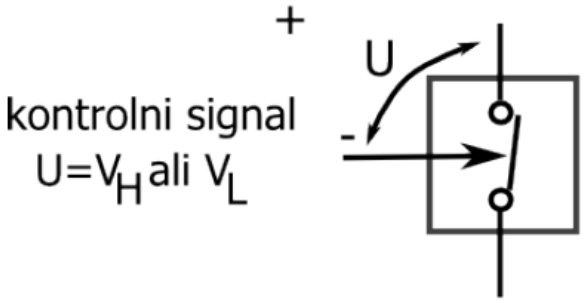
a) elektronsko stikalo: nMOS

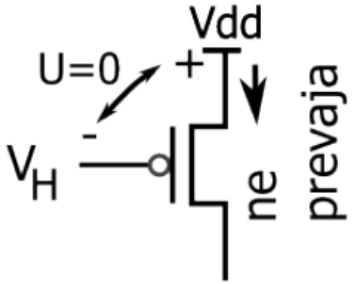


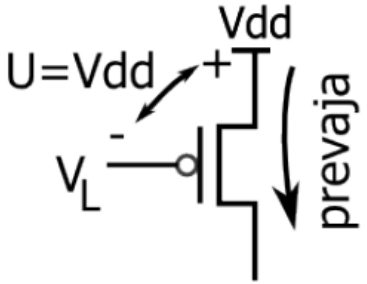




b) elektronsko stikalo: pMOS

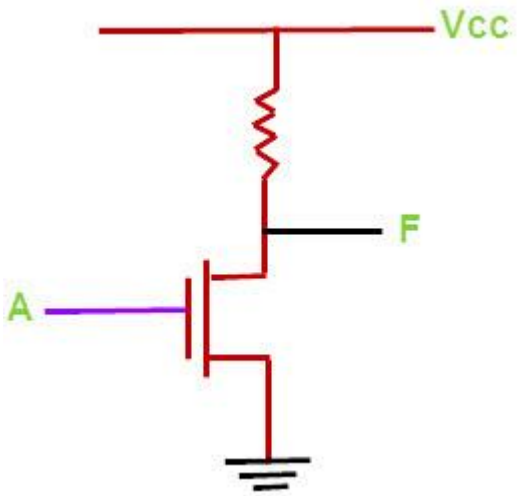


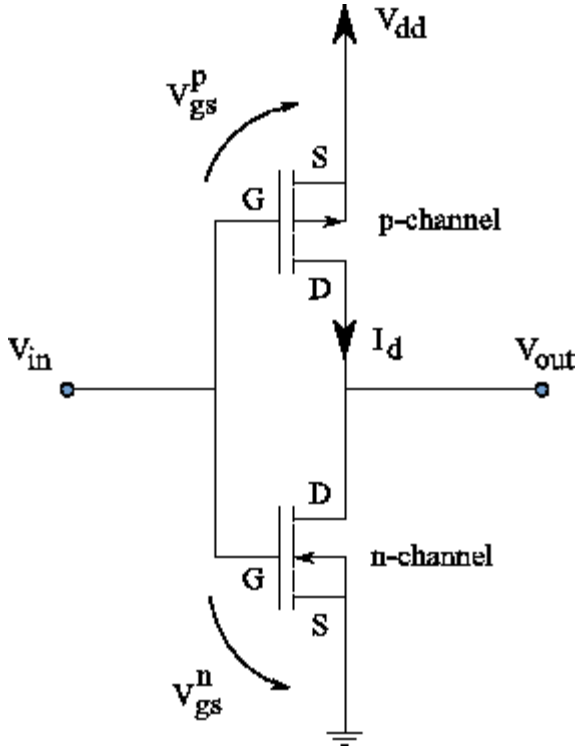




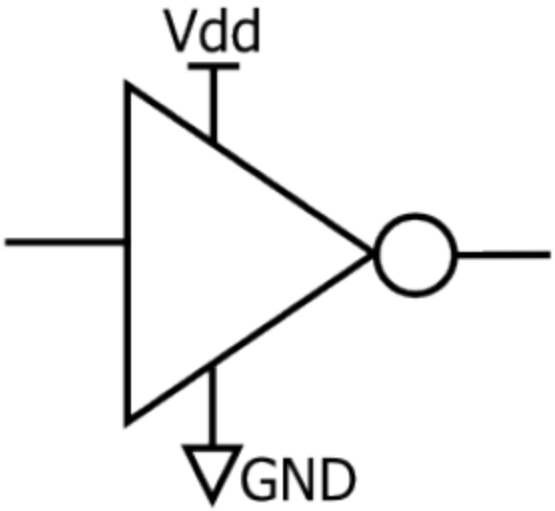
Izdelava negatorja z elektronskimi stikali

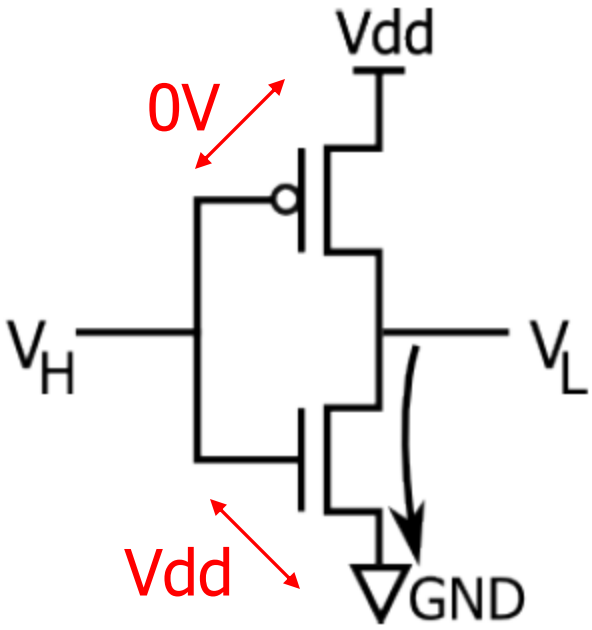
- z enim nMOS
- s pMOS in nMOS = CMOS



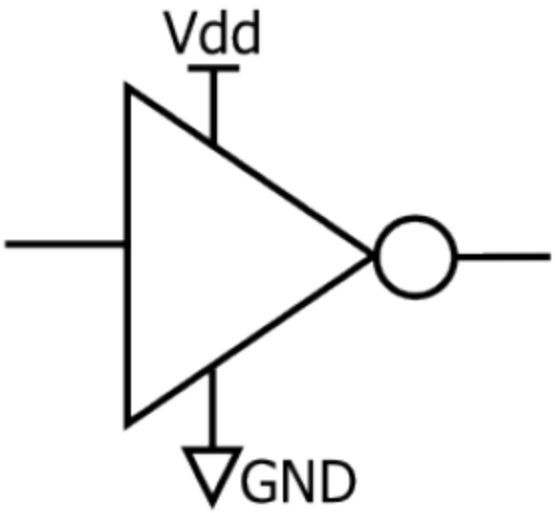


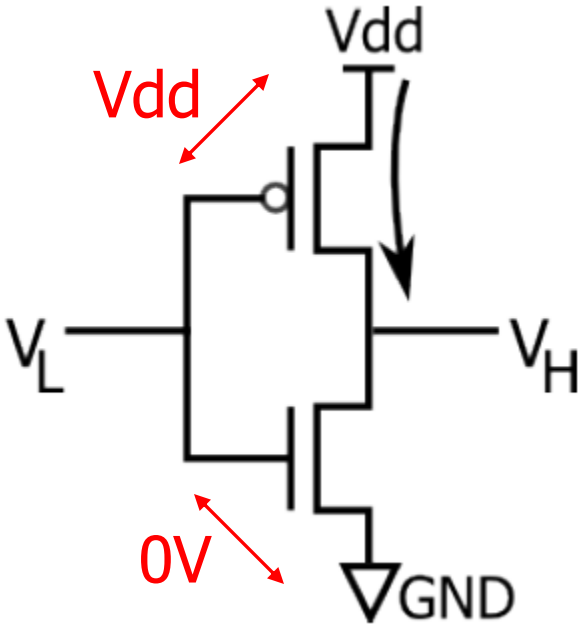
Negator v izvedbi CMOS



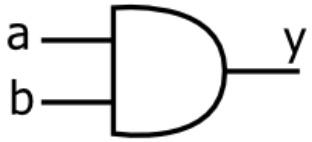
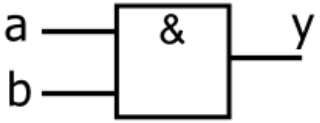
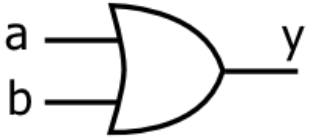
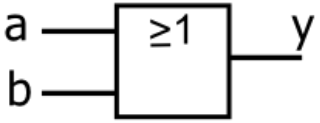
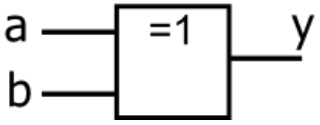


Negator v izvedbi CMOS





Logična vrata z dvema vhodoma

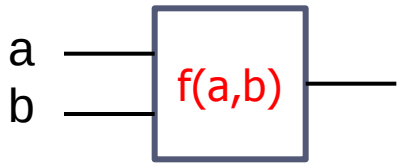
operacija	grafični simbol		pravilnostna tabela
y = a AND b	značilen:		
	IEEE:		
y = a OR b	značilen:		
	IEEE:		
y = a XOR b	značilen:		
	IEEE:		

a b | y
0 0 | 0
0 1 | 0
1 0 | 0
1 1 | 1

a b | y
0 0 | 0
0 1 | 1
1 0 | 1
1 1 | 1

a b | y
0 0 | 0
0 1 | 1
1 0 | 1
1 1 | 0

Boolove funkcije z dvema vhodoma



a	b	16 možnih funkcij															
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

a AND b

a XOR b

a OR b

NOT(a OR b)

a = b

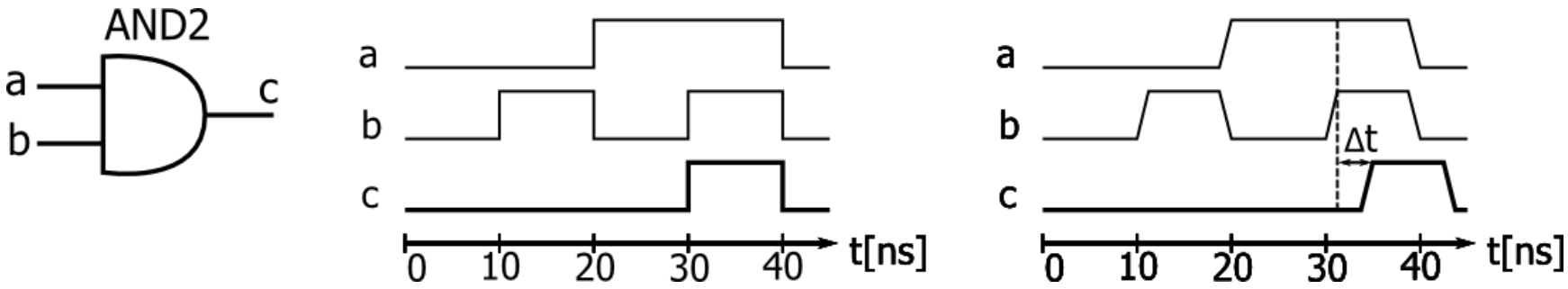
NOT b

NOT a

NOT (a AND b)

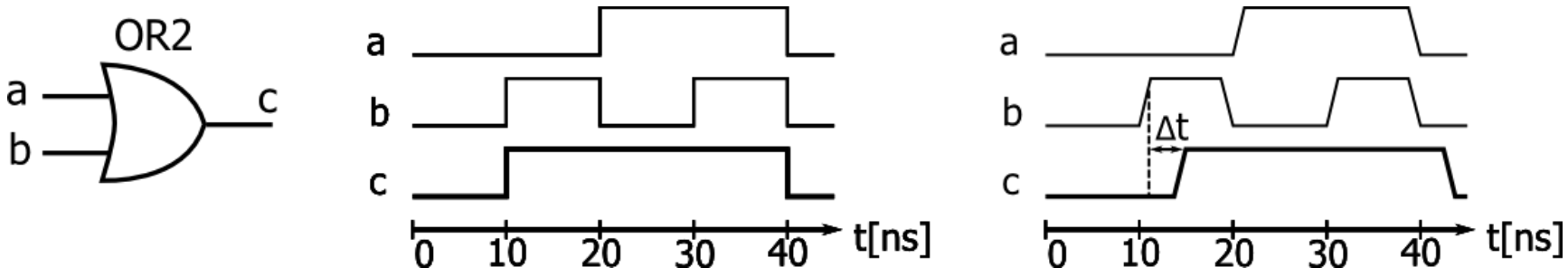
Časovni diagram logičnih vrat AND

- Simulacijski (idealni) in realni časovni diagram



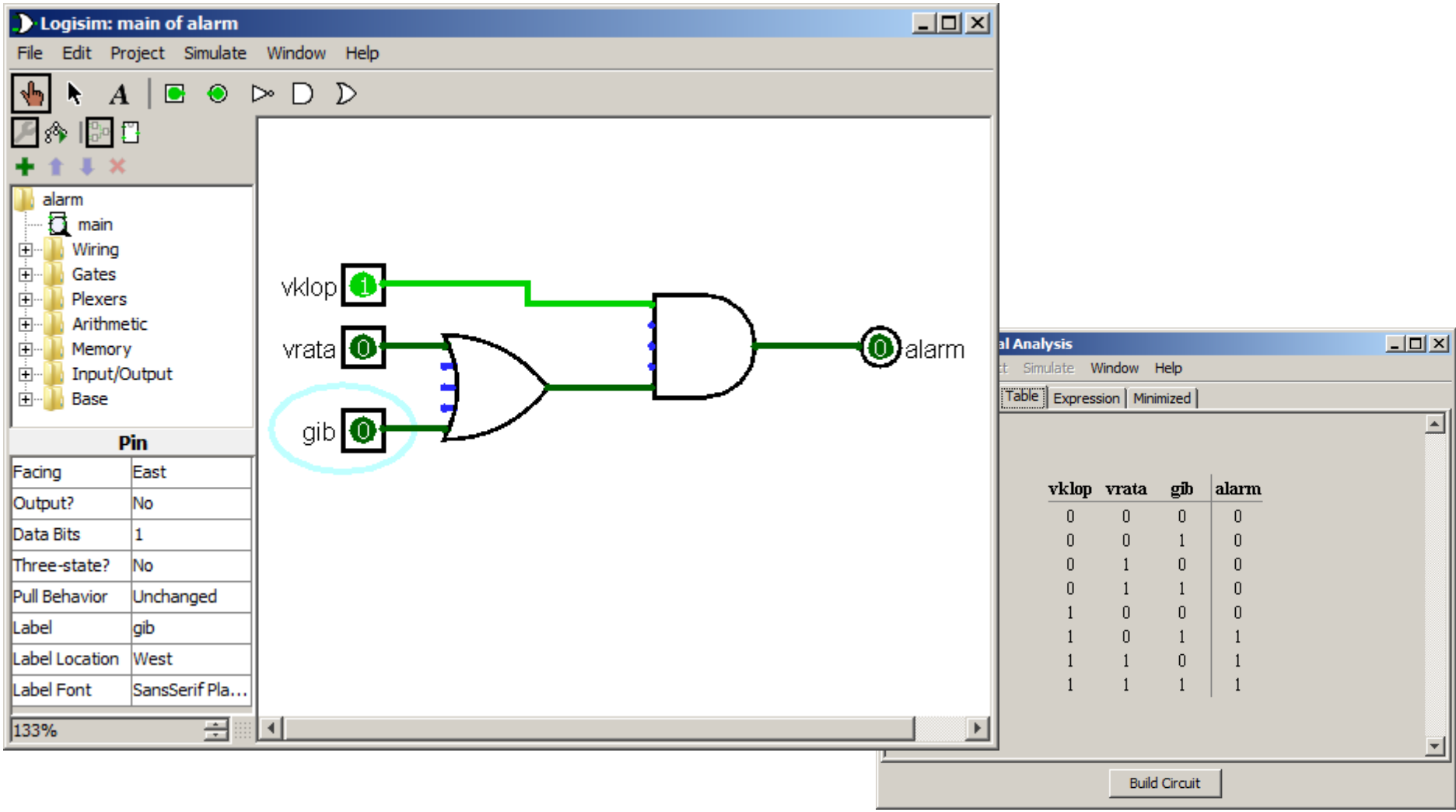
Časovni diagram logičnih vrat OR

- Simulacijski (idealni) in realni časovni diagram



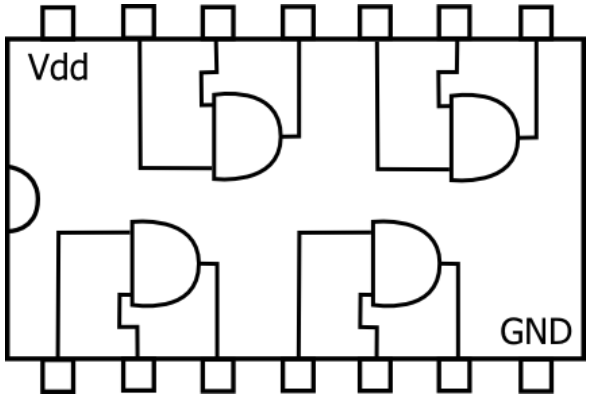
Simulator logičnih vezij

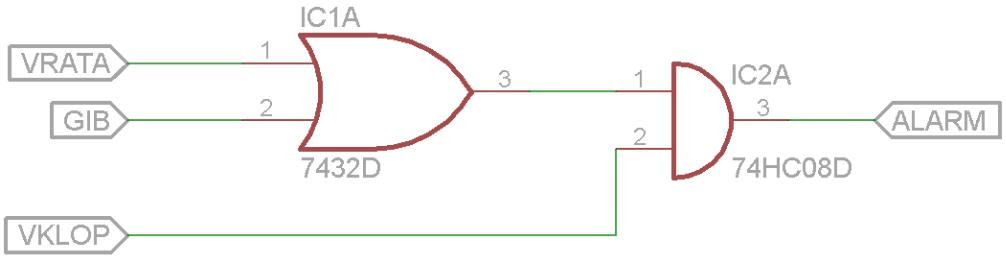
- Brezplačni programi: Logisim, LogicCircuit

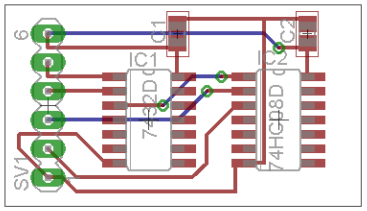


Izdelava vezij z logičnimi vrati

- Integrirana vezja s posameznimi vrati iz družine 7400
  - npr. 7408 vsebuje 4 logična vrata AND







Povzetek

- Predstavi logična vrata z dvema vhodoma (AND, OR in XOR).

- Iz katerih elektronskih elementov so sestavljena logična vrata v tehnologiji CMOS?