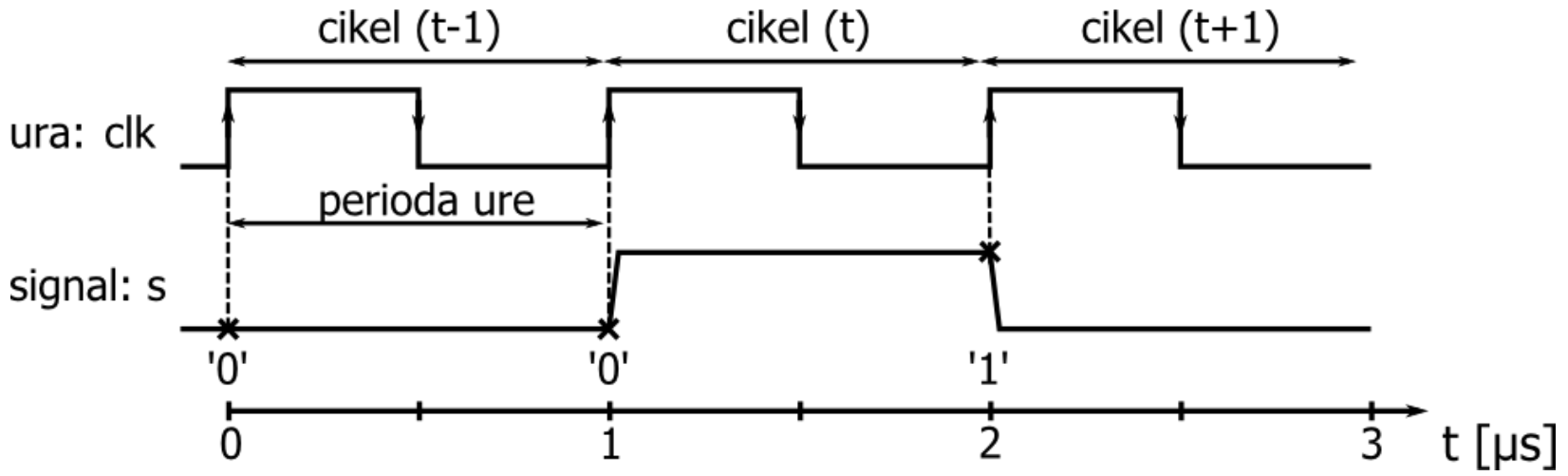
Ura in sekvenčna vezja

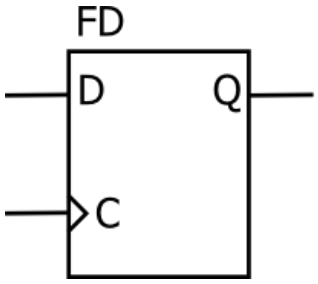
- signal, ki določa časovne trenutke spreminjanja stanja vezja
  - cikel = perioda ure, frekvenca je obratna vrednost periode
  - prehod iz 0 na 1: prednja ali naraščajoča fronta
  - prehod iz 1 na 0: zadnja ali padajoča fronta

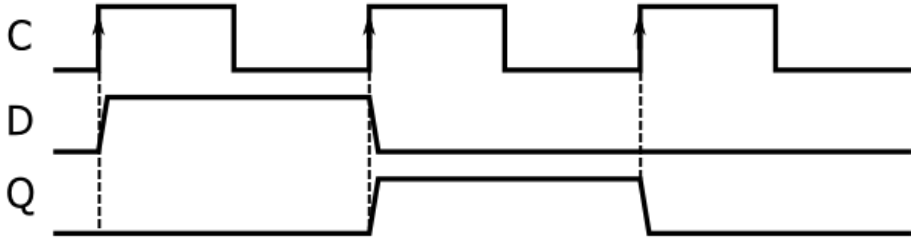


- v sekvenčnem vezju se signali spreminjajo ob prehodu ure, vmes pa imajo stabilno logično stanje

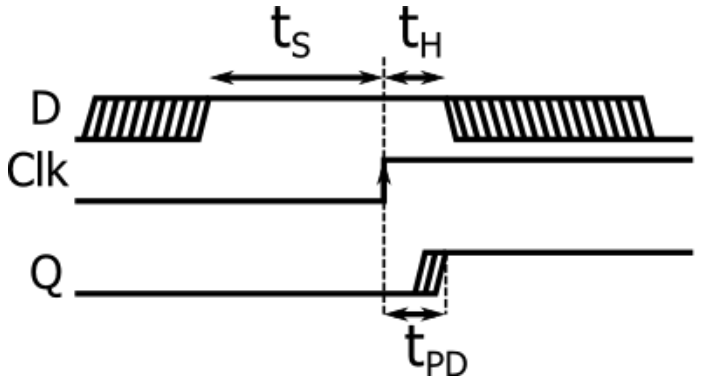
Flip-flop D

- flip-flop je pomnilni element, ki spreminja izhod ob fronti ure
- podatkovni (data) flip-flop DFF: Q(t) = D(t-1)



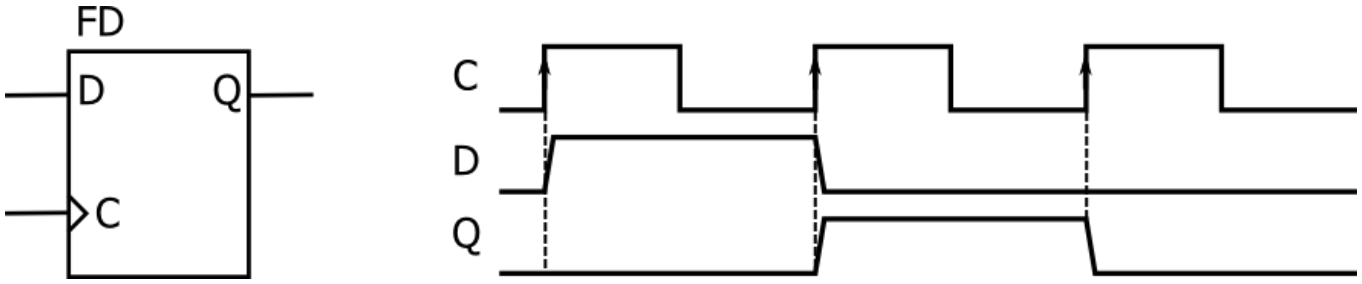


- realni časovni parametri:
  - podatkovni vhod mora biti stabilen t_S+t_H
  - izhod je zakasnjen t_{PD}

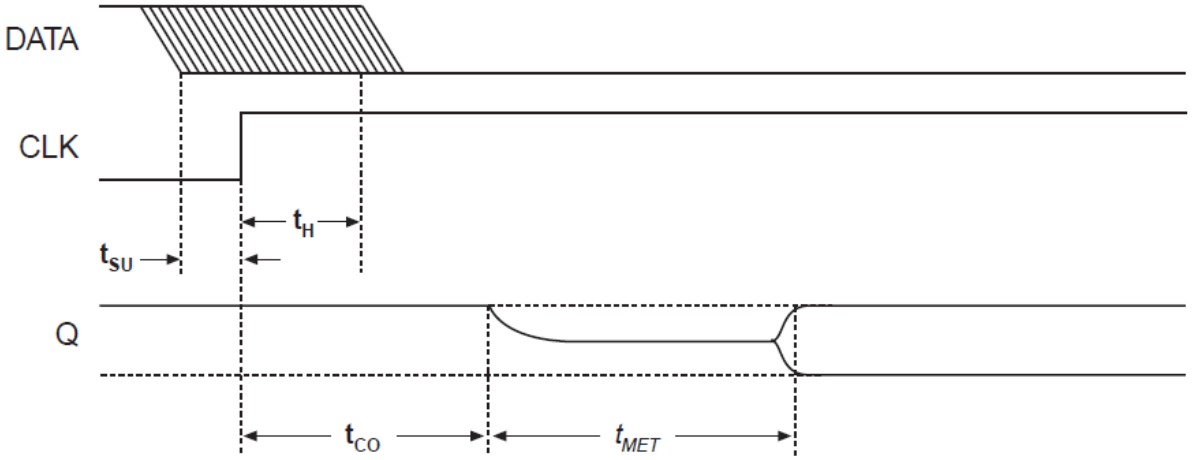


Flip-flop D

- flip-flop je pomnilni element, ki spreminja izhod ob fronti ure
- podatkovni (data) flip-flop DFF: Q(t) = D(t-1)



- če se vhod spreminja ob fronti ure lahko pride do metastabilnega stanja



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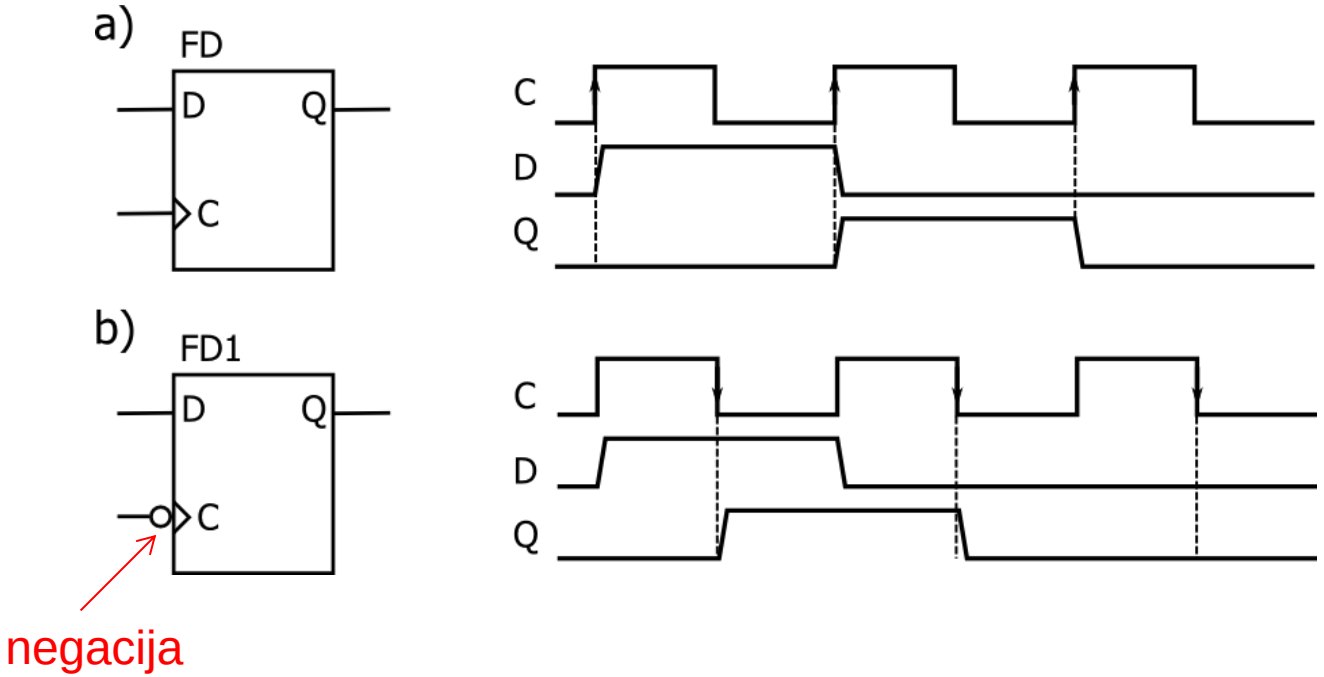
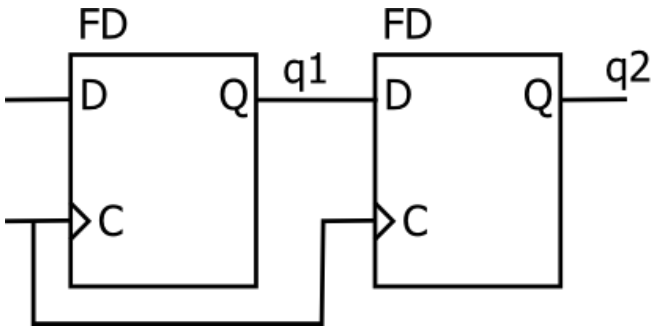
Flip-flop D

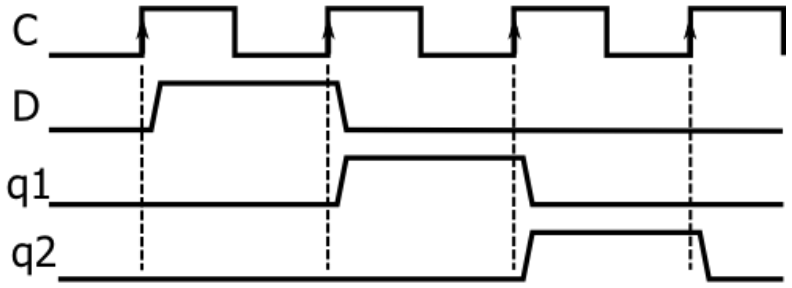
- flip-flop D preklaplja izhodni signal
  a) na prednjo fronto ali
  b) na zadnjo fronto ure



Zakasnitev signalov čez flip-flope

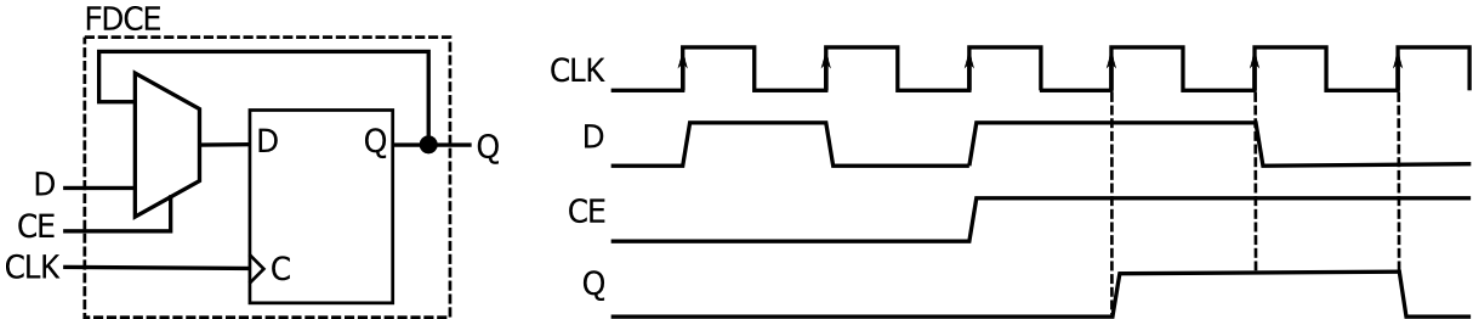
- pri prehodu čez zaporedne flip-flope se signali zakasnijo



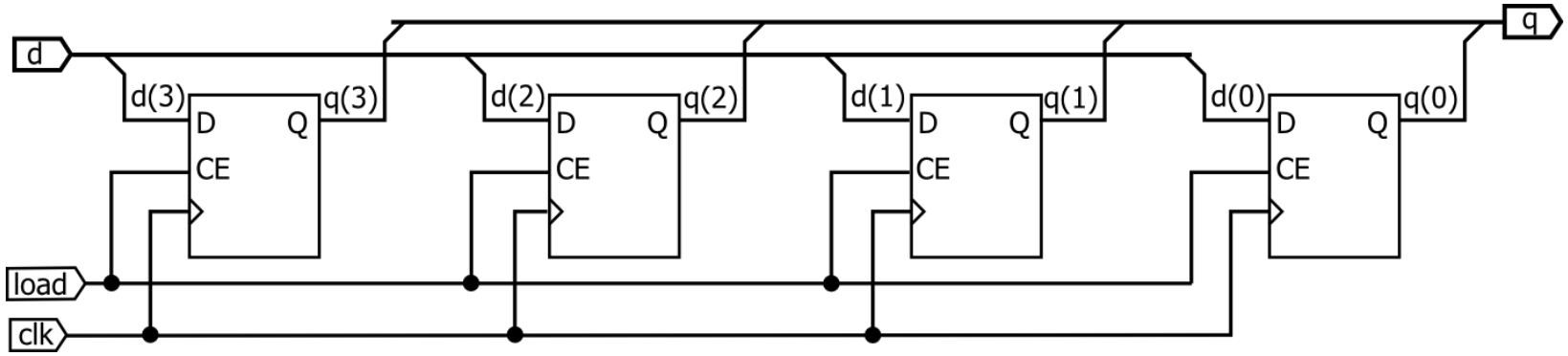


Register

- register shrani vpisano vrednost: Q(t) = Q(t-1)
  - ob fronti ure in signalu CE (Clock Enable) naloži novo vrednost
  - enobitni register – flip flop s signalom CE (FDCE)

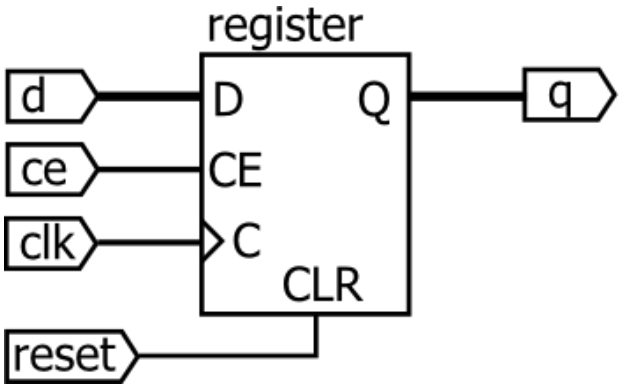


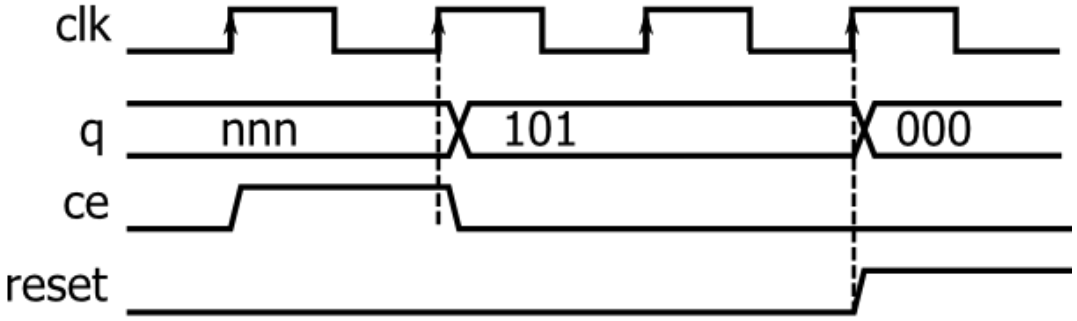
- shema 4-bitnega registra



Izvedbe registrov

- register s signalom reset



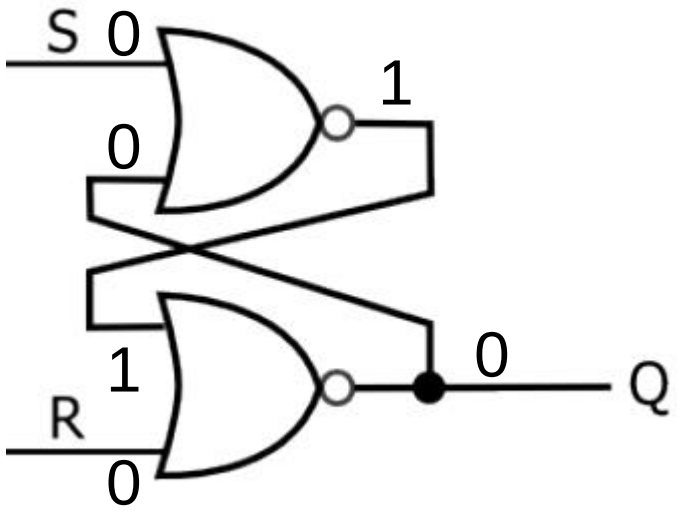


Izdelava pomnilnih gradnikov

- pomnilni gradniki so sestavljeni iz logičnih vrat s povratno vezavo
  - zapah SR lahko shrani (zapahne) vrednost izhoda

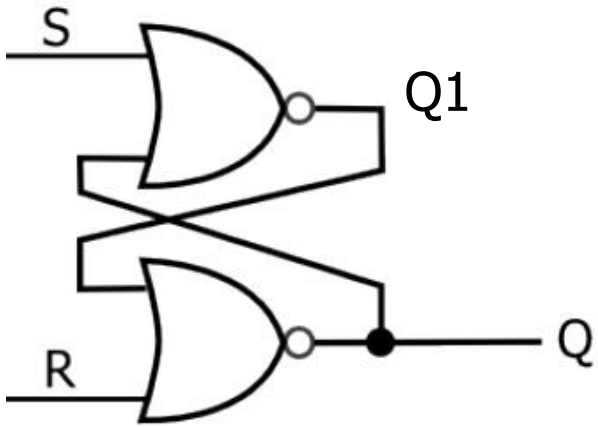
Zapah

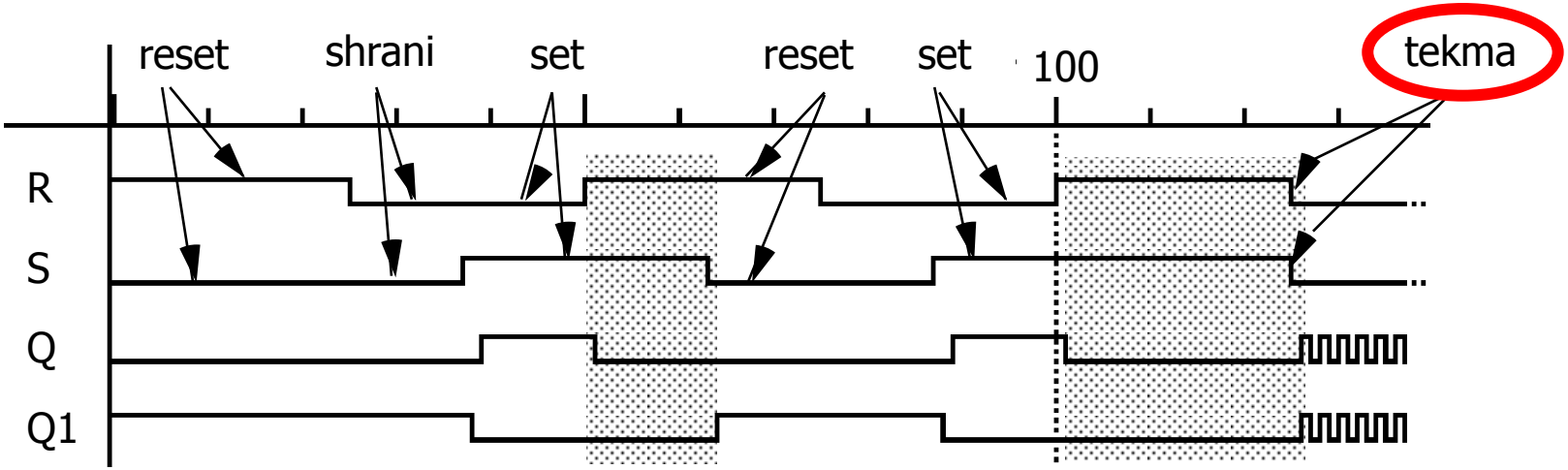
S=1, Q=1
R=1, Q=0
S=0, R=0, Q=Q



Izdelava pomnilnih gradnikov

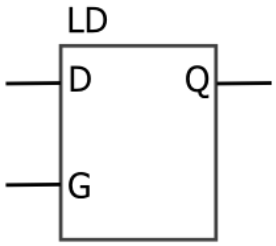
- zapah RS je lahko nestabilen
  - kadar sta R in S na 1 in gresta hkrati nazaj na 0

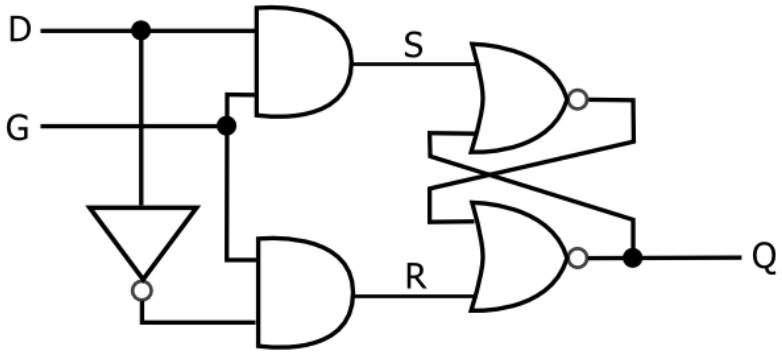


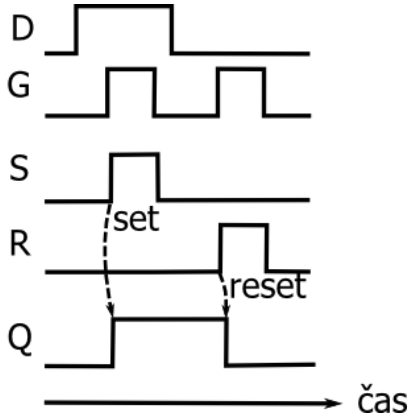


Rešitev: podatkovni zapah

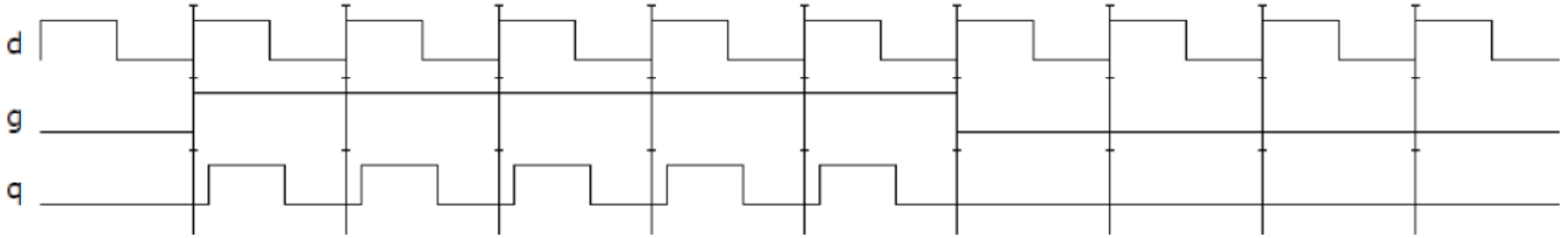
- dodatna logika prepreči, da sta R in S na 1
- zapah D – kadar je ura G=0 ohranja stanje





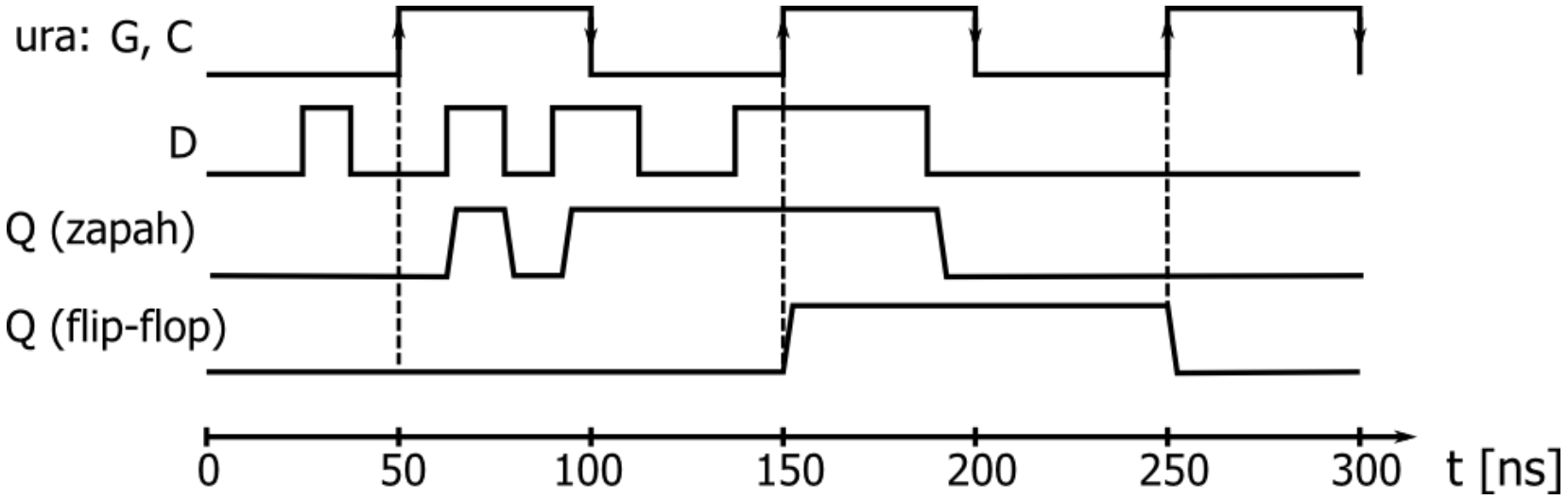


- kadar je G=1 je zapah transparenten

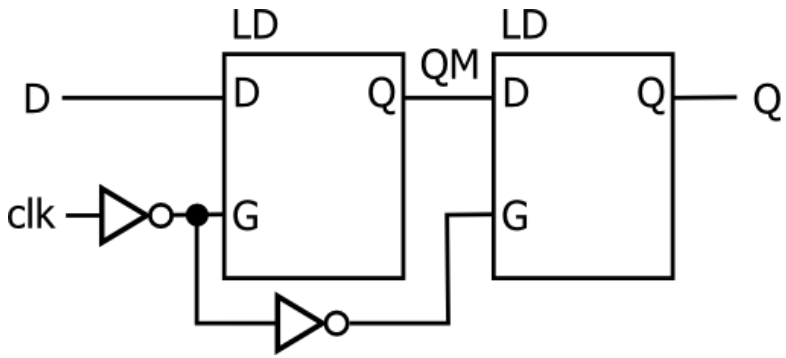


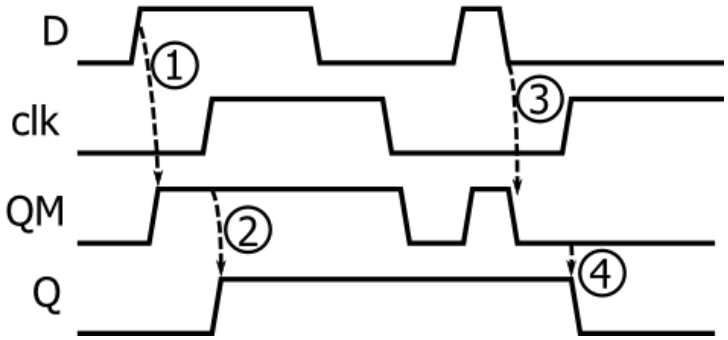
Podatkovni zapah in flip-flop

- zapah D – kadar je ura na 0 ohranja stanje
- flip-flop – ohranja stanje cel urni cikel, spreminja pa le ob fronti ure



Flip-flop D

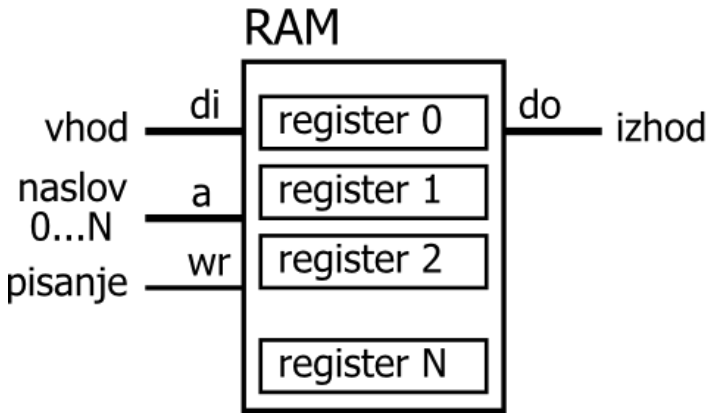


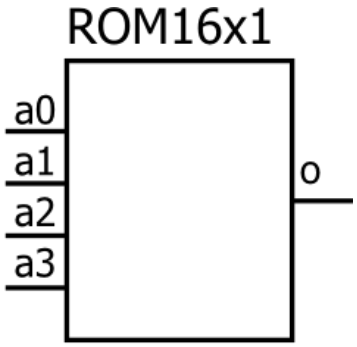


- (1) prvi zapah prenese D na QM
- (2) ob fronti ure se QM zapahne in prenese na Q
- (3) sprememba D ob clk=0 se ne prenese na izhod
- (4) ob naslednji fronti se D prenese na Q

Pomnilnik

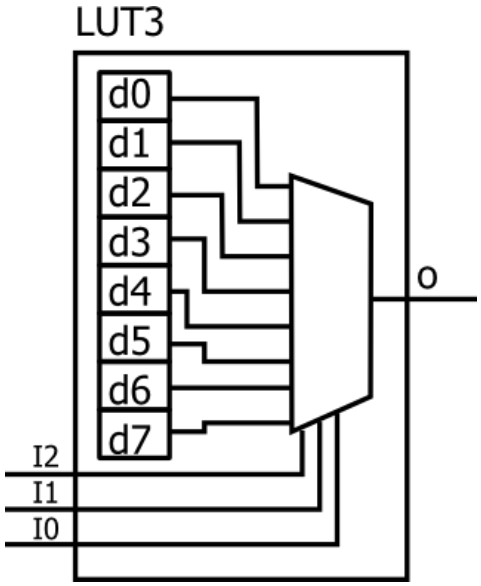
- pomnilnik shranjuje več besed
- signali:
  - podatkovni vhod in izhod (data)
  - naslovno vodilo – vsaka celica ima svoj naslov (address)
  - krmilni – branje, pisanje
- RAM (Random Access Memory) in ROM (Read Only Memory)



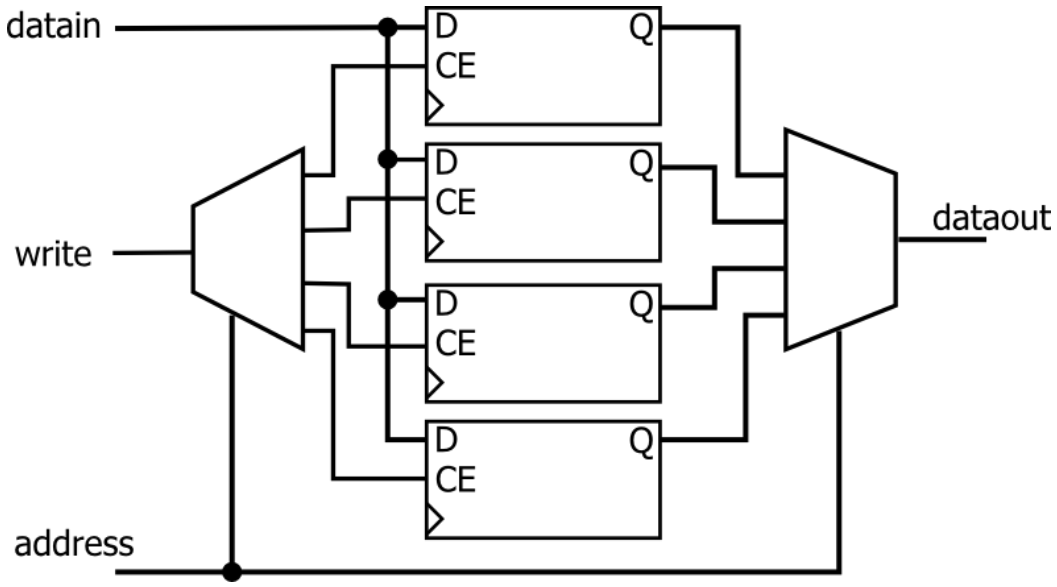


Pomnilnik ROM

- vsebino pomnilnika ROM v programirljivih vezjih določimo ob programiranju
  - takšen ROM se imenuje vpogledna tabela Look-Up Table

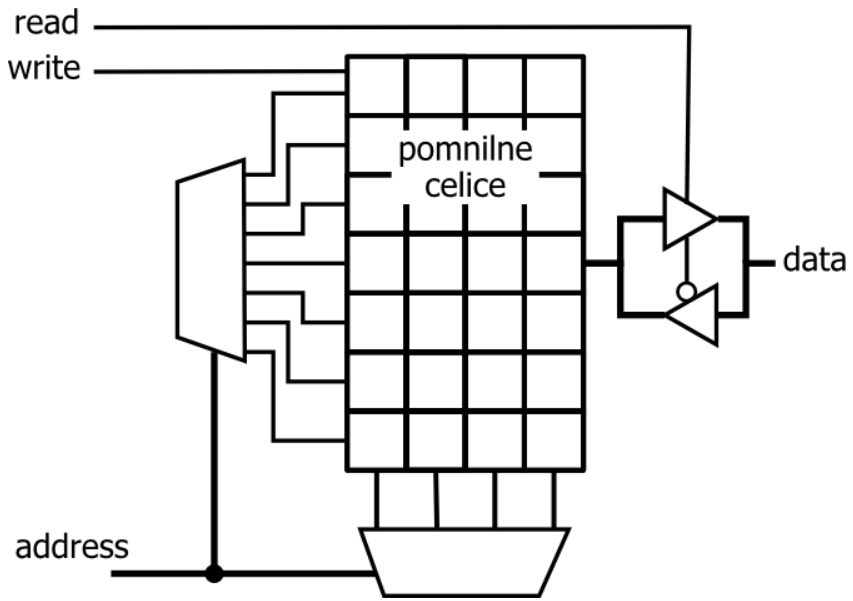


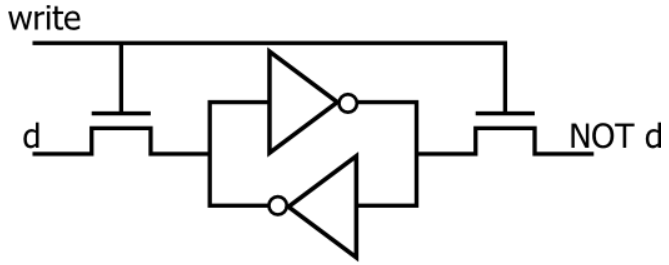
Izvedba RAM iz registrov



- registri iz flip-flopov D potrebujejo veliko transistorjev

Izvedba RAM iz pomnilnih celic





- statični pomnilnik – SRAM
- dinamični – DRAM, shrani podatek v kondenzatorju
  - potrebno je osveževati vsebino