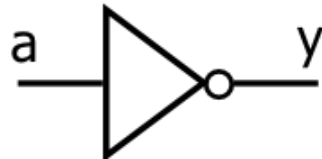


Boolova logična vrata

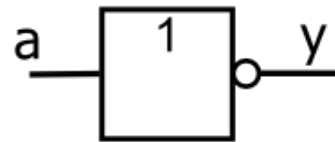
- ▶ Logične funkcije nad binarnimi vrednostmi: 0 in 1
- ▶ Najbolj preprost gradnik je negator
 - ▶ en vhodni in en izhodni signal
 - ▶ izhod ima invertirano (negirano) vrednost glede na vhod

$$y = \text{NOT}(a)$$

značilen simbol:

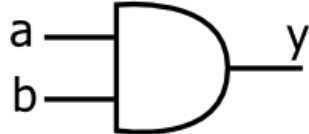
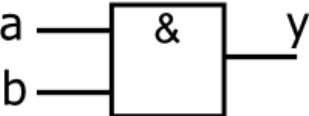
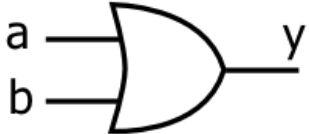
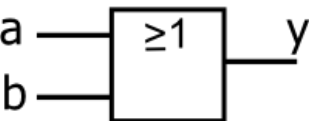
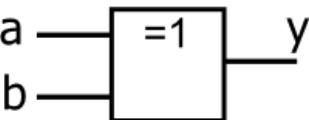


IEEE simbol:

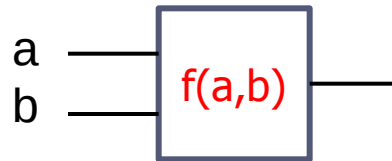


a	y
0	1
1	0

Logična vrata z dvema vhodoma

operacija	grafični simbol	pravilnostna tabela															
$y = a \text{ AND } b$	značilen: 	<table><tr><td>a</td><td>b</td><td>y</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	a	b	y	0	0	0	0	1	0	1	0	0	1	1	1
a	b	y															
0	0	0															
0	1	0															
1	0	0															
1	1	1															
	IEEE: 																
$y = a \text{ OR } b$	značilen: 	<table><tr><td>a</td><td>b</td><td>y</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	a	b	y	0	0	0	0	1	1	1	0	1	1	1	1
a	b	y															
0	0	0															
0	1	1															
1	0	1															
1	1	1															
	IEEE: 																
$y = a \text{ XOR } b$	značilen: 	<table><tr><td>a</td><td>b</td><td>y</td></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	a	b	y	0	0	0	0	1	1	1	0	1	1	1	0
a	b	y															
0	0	0															
0	1	1															
1	0	1															
1	1	0															
	IEEE: 																

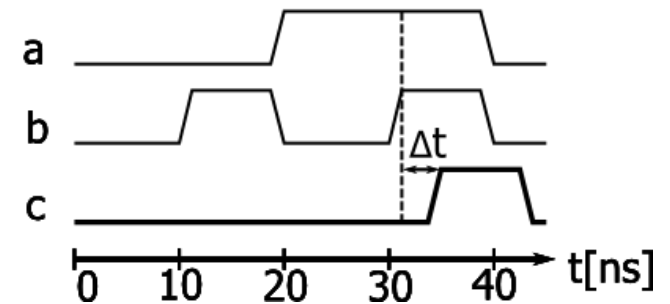
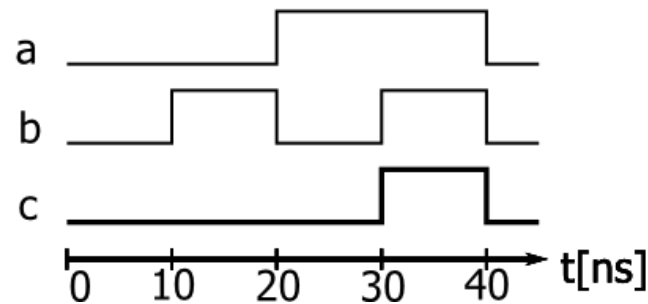
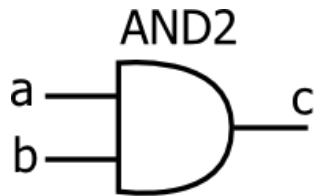
Boolove funkcije z dvema vhodoma



a	b	16 možnih funkcij															
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		a AND b				a XOR b				a OR b		a = b		NOT a		NOT (a AND b)	
										NOT(a OR b)				NOT b			

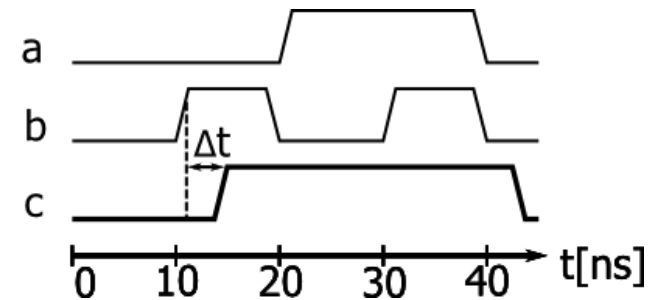
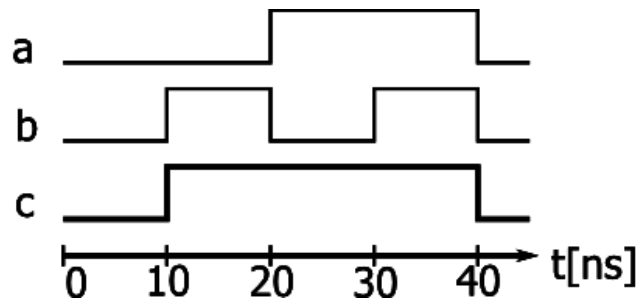
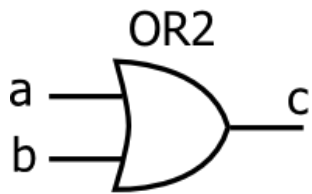
Časovni diagram logičnih vrat AND

- ▶ Simulacijski (idealni) in realni časovni diagram



Časovni diagram logičnih vrat OR

- Simulacijski (idealni) in realni časovni diagram



Simulator logičnih vezij

► Risanje in simulacija vezja v orodju Logisim

Logisim: main of alarm

File Edit Project Simulate Window Help

vklop 1

vrata 0

gib 0

alarm 0

Pin

Facing	East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	gib
Label Location	West
Label Font	SansSerif Pla...

133%

Logic Analysis

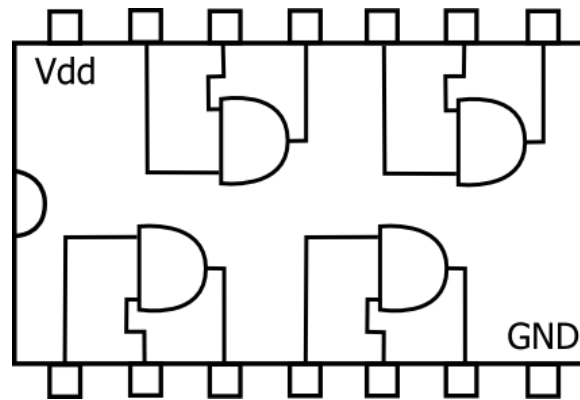
Table Expression Minimized

vklop	vrata	gib	alarm
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Build Circuit

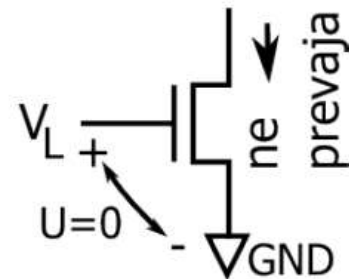
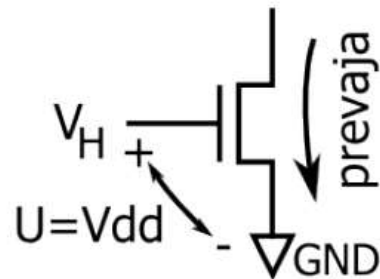
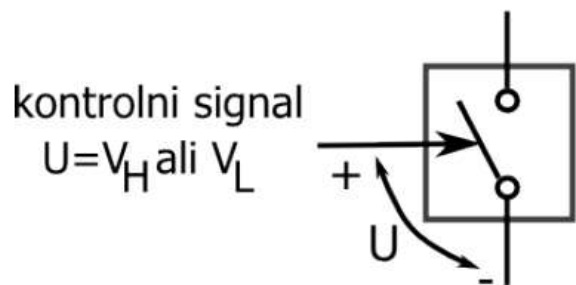
Izdelava logičnih vrat

- ▶ Integrirana vezja s posameznimi vrati iz družine 74nnn
 - ▶ npr. 7408 vsebuje 4 logična vrata AND

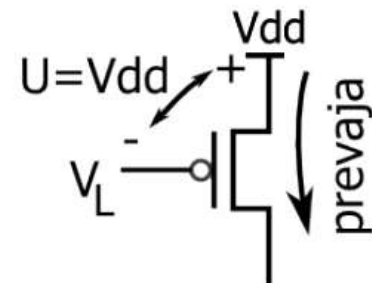
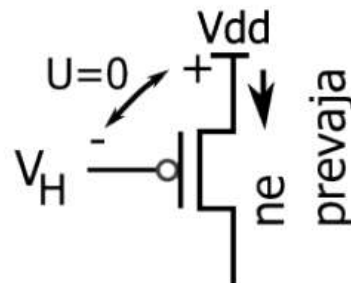
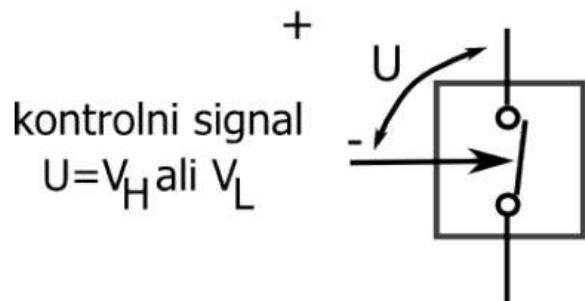


Elektronska stikala

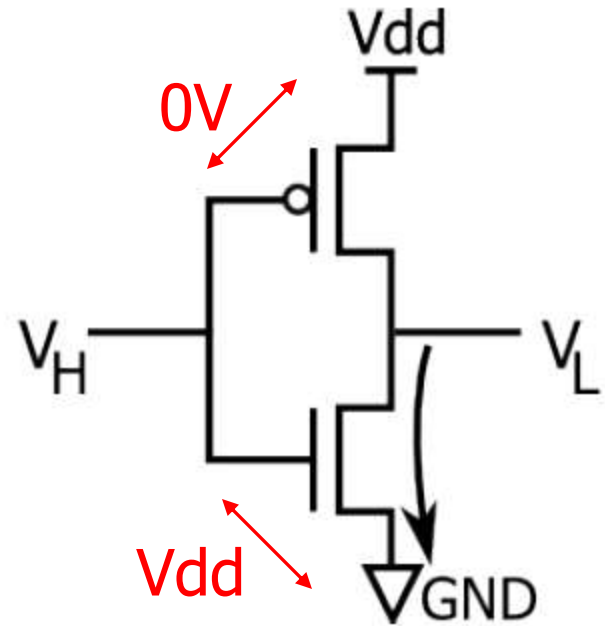
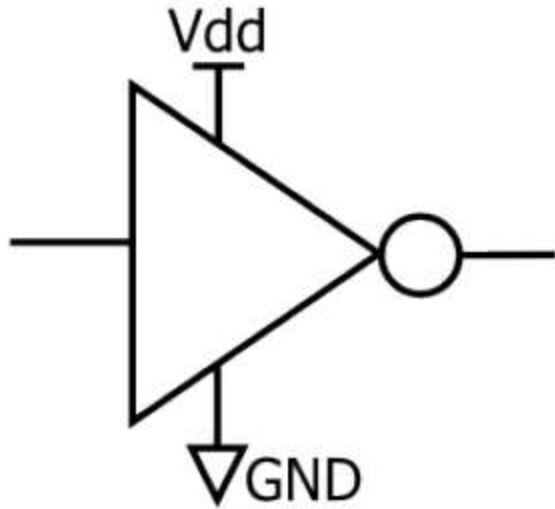
a) elektronsko stikalo: nMOS



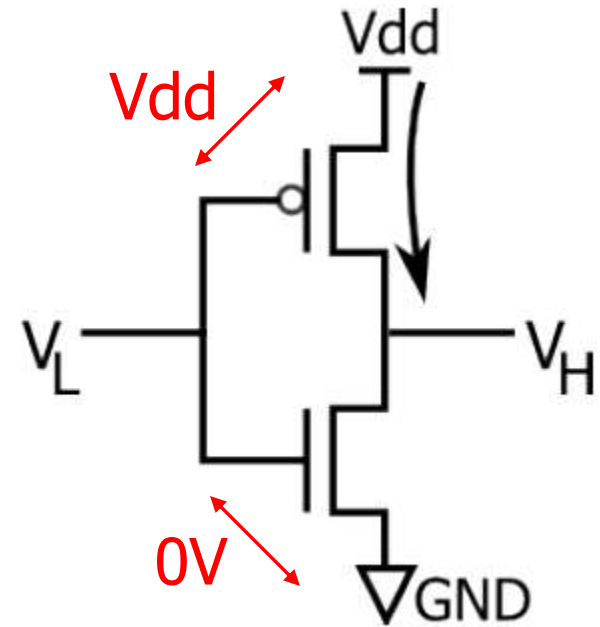
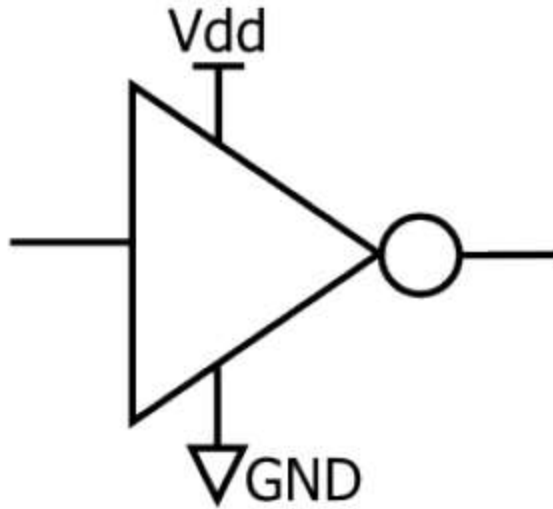
b) elektronsko stikalo: pMOS



Negator v izvedbi CMOS

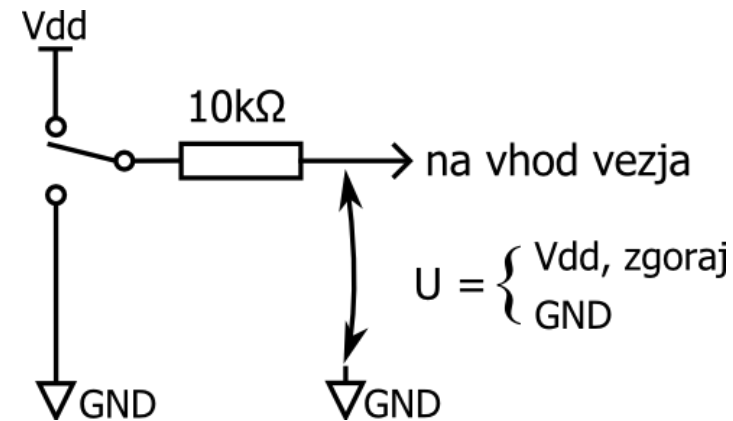


Negator v izvedbi CMOS



Signali v integriranih vezjih

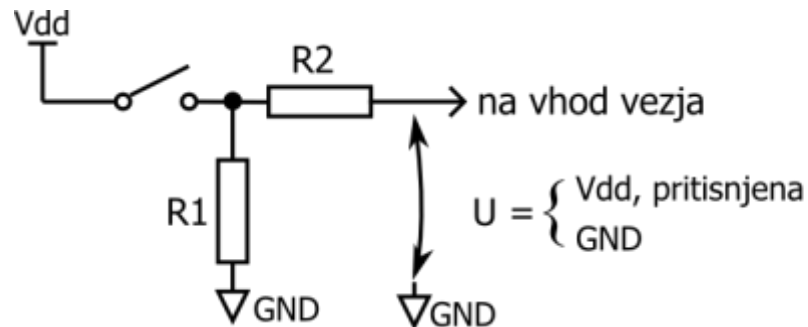
- ▶ Priključki na programirljivih vezjih so običajno dvosmerni
 - ▶ ko oblikujemo vezje, določimo ali je vhod ali izhod
- ▶ Kadar je priključek vhod ima zelo veliko upornost
- ▶ Kadar je izhod pa ima majhno notranjo upornost proti Vdd ali GND
 - ▶ poskrbeti moramo, da vežemo izhoda na Vdd ali GND, ker bi naredili kratek stik
- ▶ Primer: vezava preklopnega stikala
 - ▶ v serijo vežemo zaščitni upor



Vezava tipke

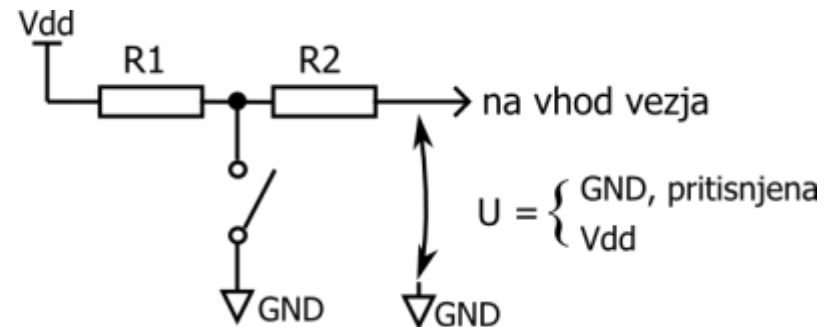
- Potrebujemo predupor R1, ki določa logično stanje ko je tipka spuščena in zaščitni upor R2 (vrednosti nekaj k Ω)

Pozitivna logika



- na vhod vezja '1' ko je tipka pritisnjena

Negativna logika

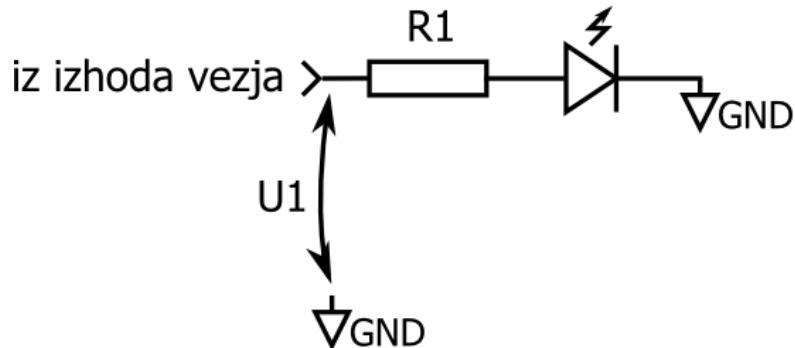


- na vhod vezja '0' ko je tipka pritisnjena

Vezava svetleče diode - LED

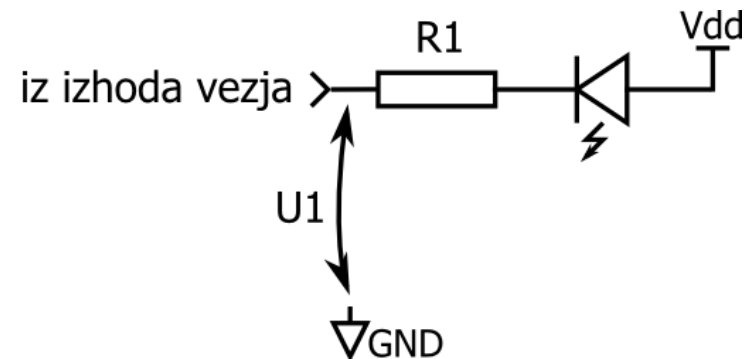
- ▶ Potrebujemo predupor R1 za omejitev toka skozi LED
 - ▶ npr. za 3.3mA LED izračunamo $(3.3V - 2V) / 3.3mA = 390\Omega$

Pozitivna logika



- ▶ LED sveti, ko je na izhodu vezja '1'

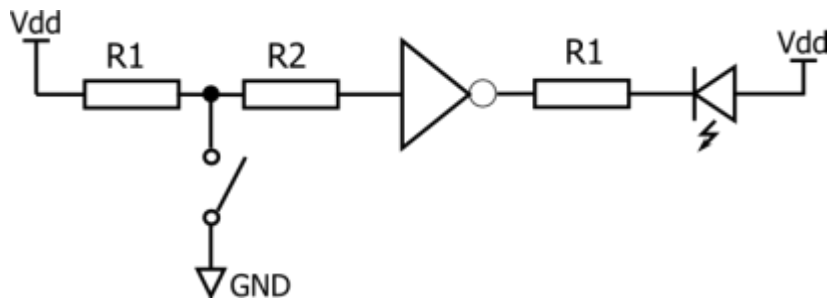
Negativna logika



- ▶ LED sveti, ko je na izhodu vezja '0'

Kdaj bo LED prižgana?

Ko bo tipka razklenjena.



Ne glede na tipko!

