# Sistem na čipu Zynq in Vivado

Vivado, VHDL model, simulacija, sinteza

blokovni načrt, priključki, prevajanje

Andrej Trost

Laboratorij za načrtovanje integriranih vezij

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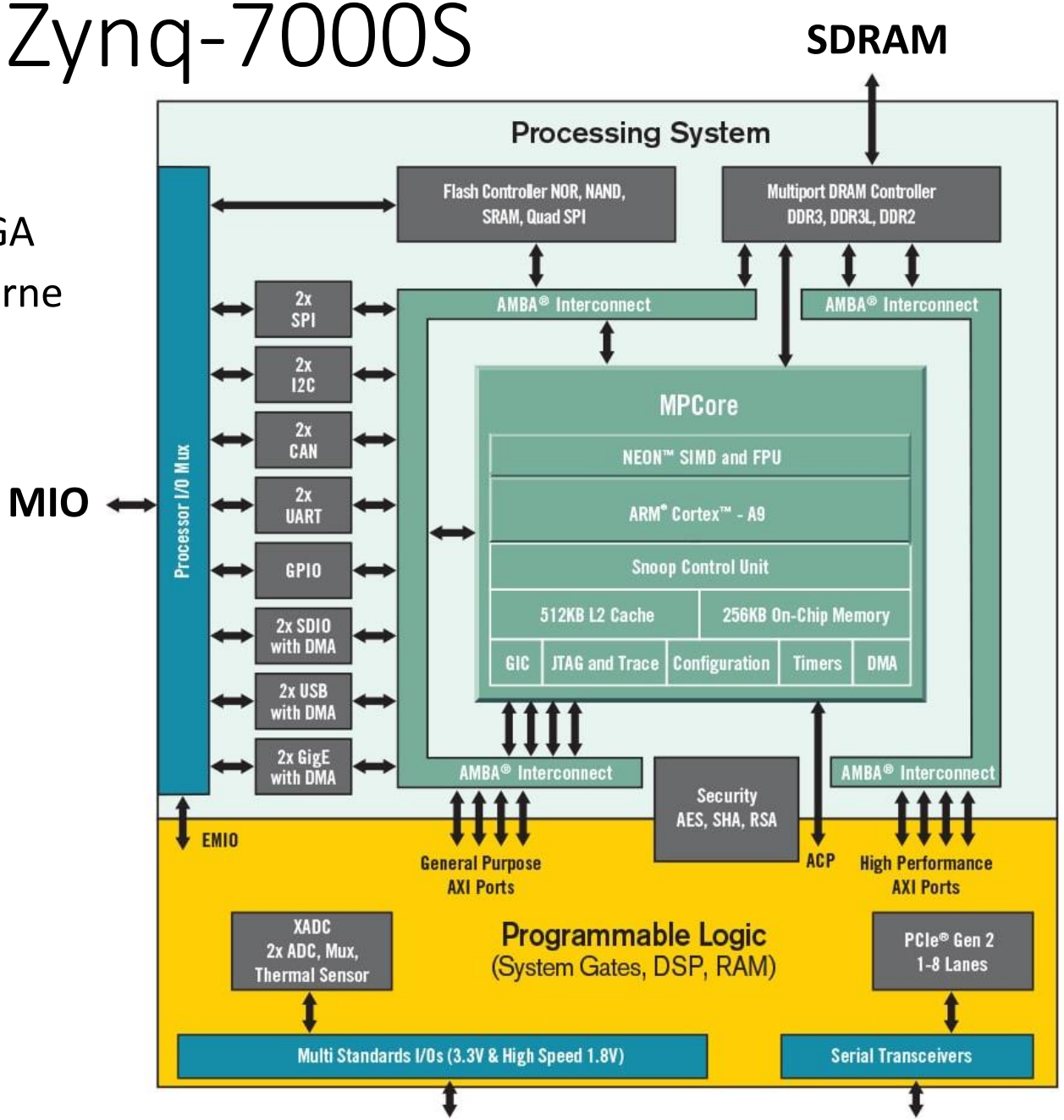
# AMD-Xilinx Zynq-7000S

- Sistem na čipu (SoC)
  - ARM Cortex-A9 in FPGA
  - multipleksirane periferne enote (MIO)
  - na FPGA povezani vmesniki AXI



# Razvojne plošče

MiniZed

- XC7Z007S
  Artix-7 + ARM Cortex-A9
  14k LUT / 29k FF
  66 DSP48
  50 BRAM (36k)
  XADC
- DDR3, Flash, eMMC
- USB, Wi-Fi, BLE
- senzor gibanja, temp
  mikrofon

Cora Z7-07S


Red Pitaya

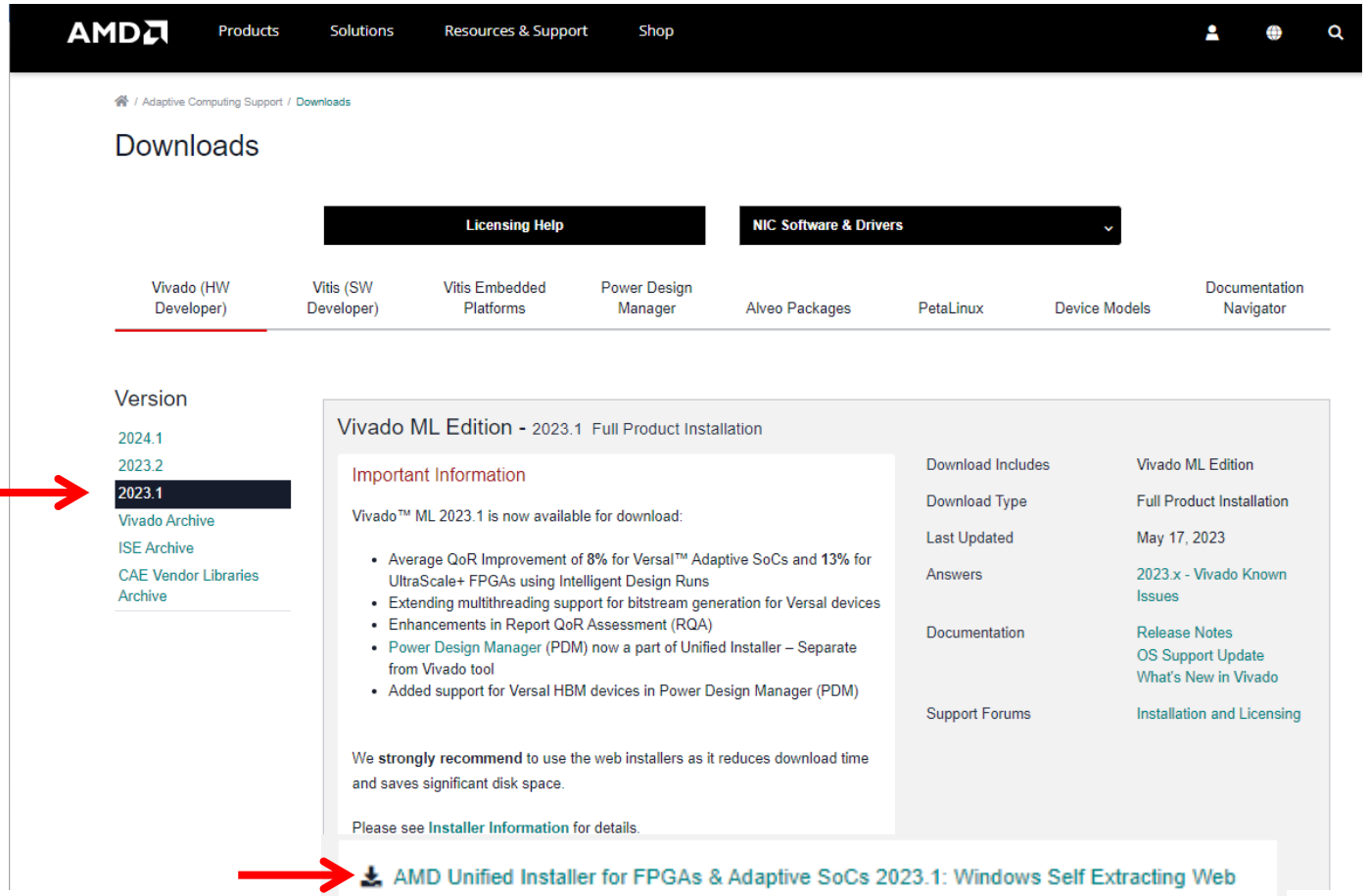
- XC7Z010
  2xARM Cortex-A9
  17k LUT / 35k FF
  80 DSP48
  60 BRAM
- AD/DA 125 Msps
- Linux

ZedBoard

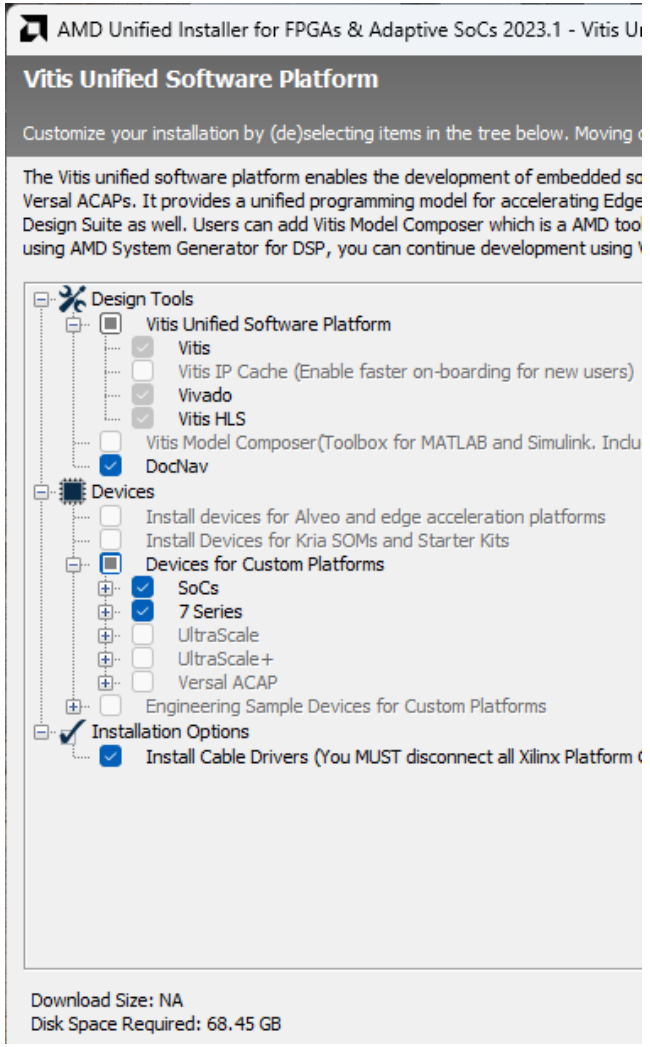

- XC7Z020
  2xARM Cortex-A9
  53k LUT / 106k FF
  220 DSP48
  140 BRAM

# Namestitev Vivado 2023.1

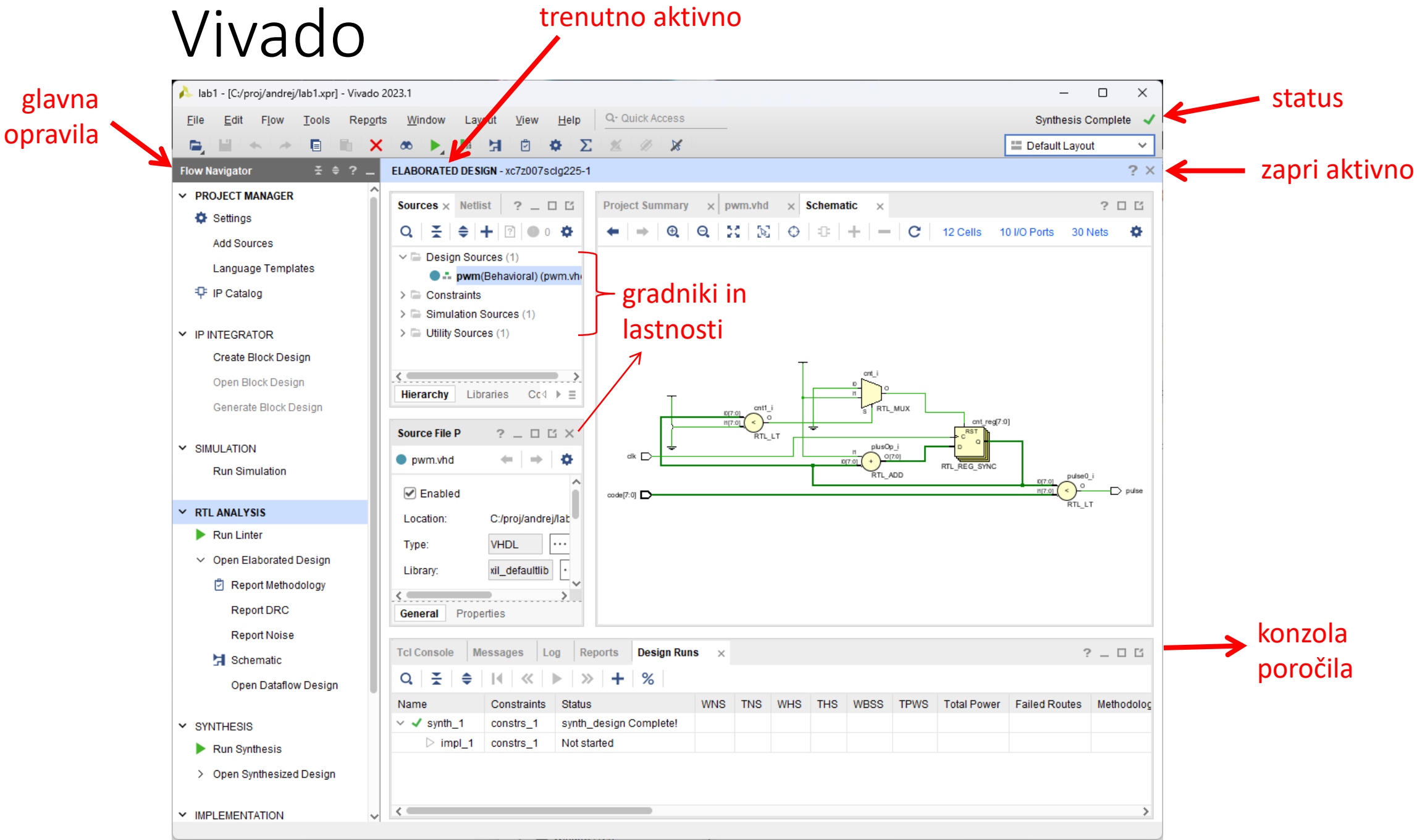
https://www.xilinx.com/support/download.html



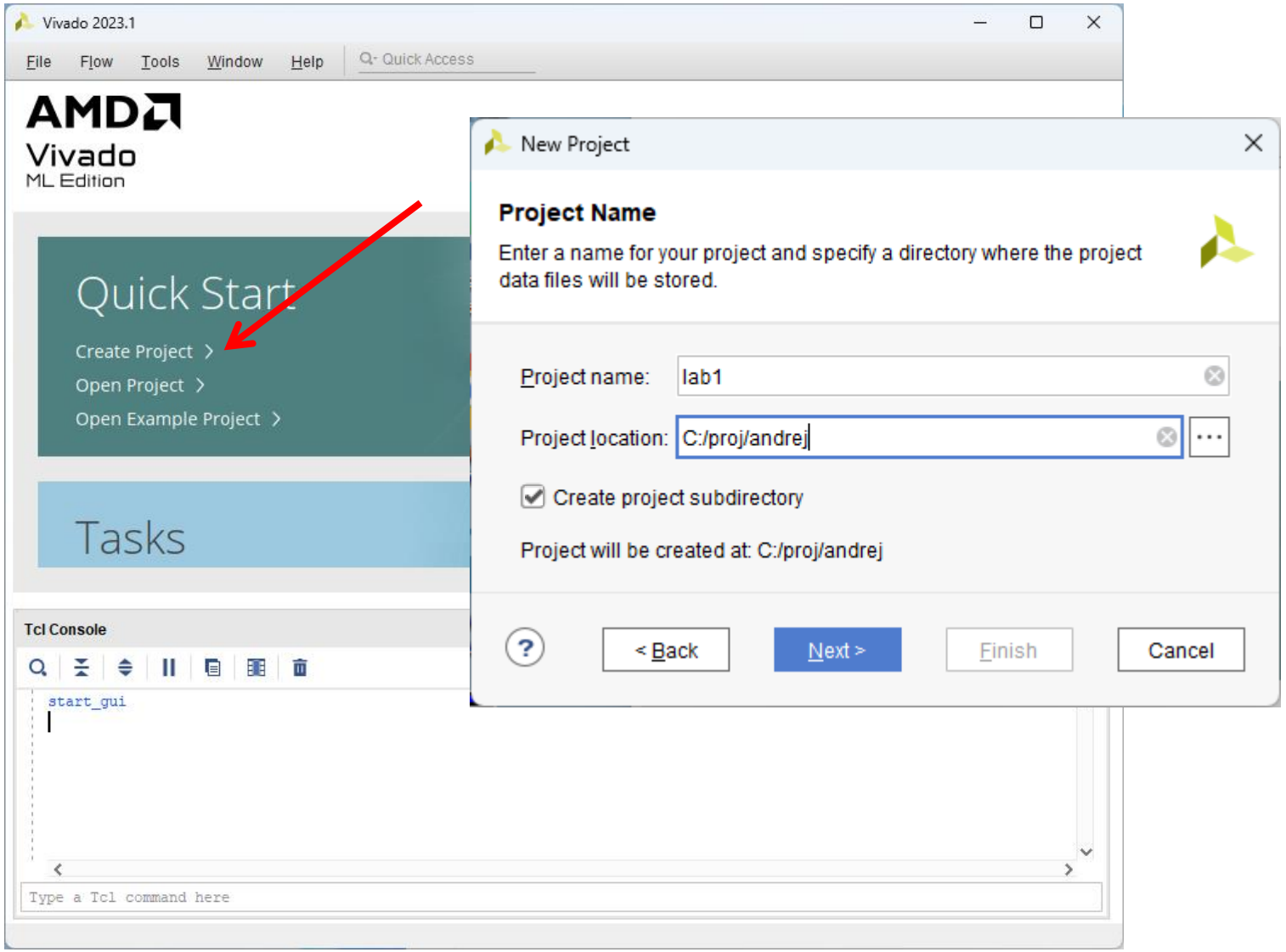

Select Product:
o **Vitis**



# Vivado

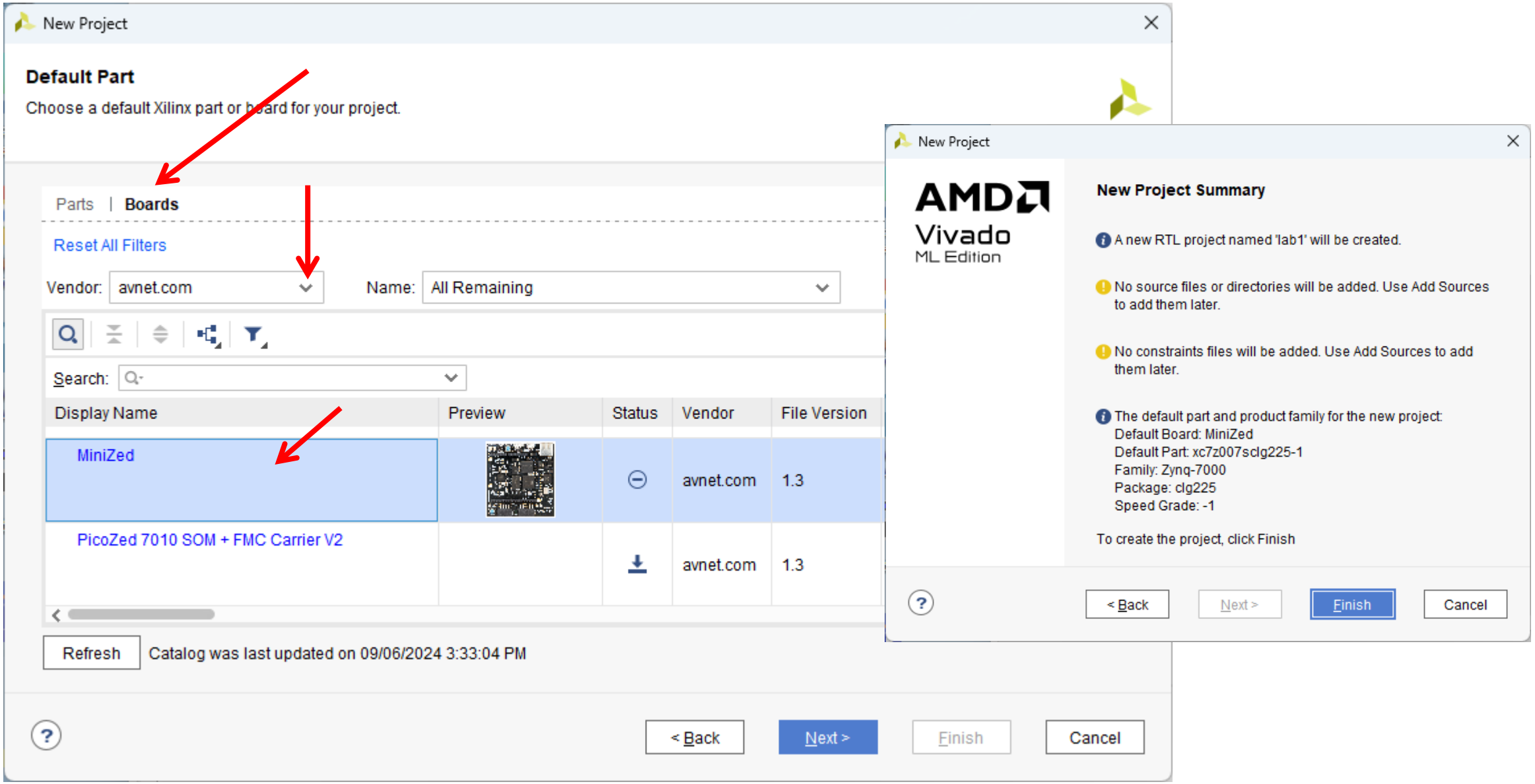

trenutno aktivno
glavna opravila
status
zapri aktivno
gradniki in lastnosti
konzola poročila
lab1 - [C:/proj/andrej/lab1.xpr] - Vivado 2023.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
Open Dataflow Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
ELABORATED DESIGN - xc7z007sclg225-1
Sources
Netlist
Design Sources (1)
pwm(Behavioral) (pwm.vh
Constraints
Simulation Sources (1)
Utility Sources (1)
Hierarchy
Libraries
Source File P
pwm.vhd
Enabled
Location:
Type:
VHDL
Library:
xil_defaultlib
General
Properties
Project Summary
pwm.vhd
Schematic
12 Cells
10 I/O Ports
30 Nets
RTL_MUX
RTL_LT
RTL_ADD
RTL_REG_SYNC
clk
code[7:0]
pulse
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
WBSS
TPWS
Total Power
Failed Routes
synth_1
constrs_1
synth_design Complete!
impl_1
constrs_1
Not started

# Vivado 2023 - nov projekt

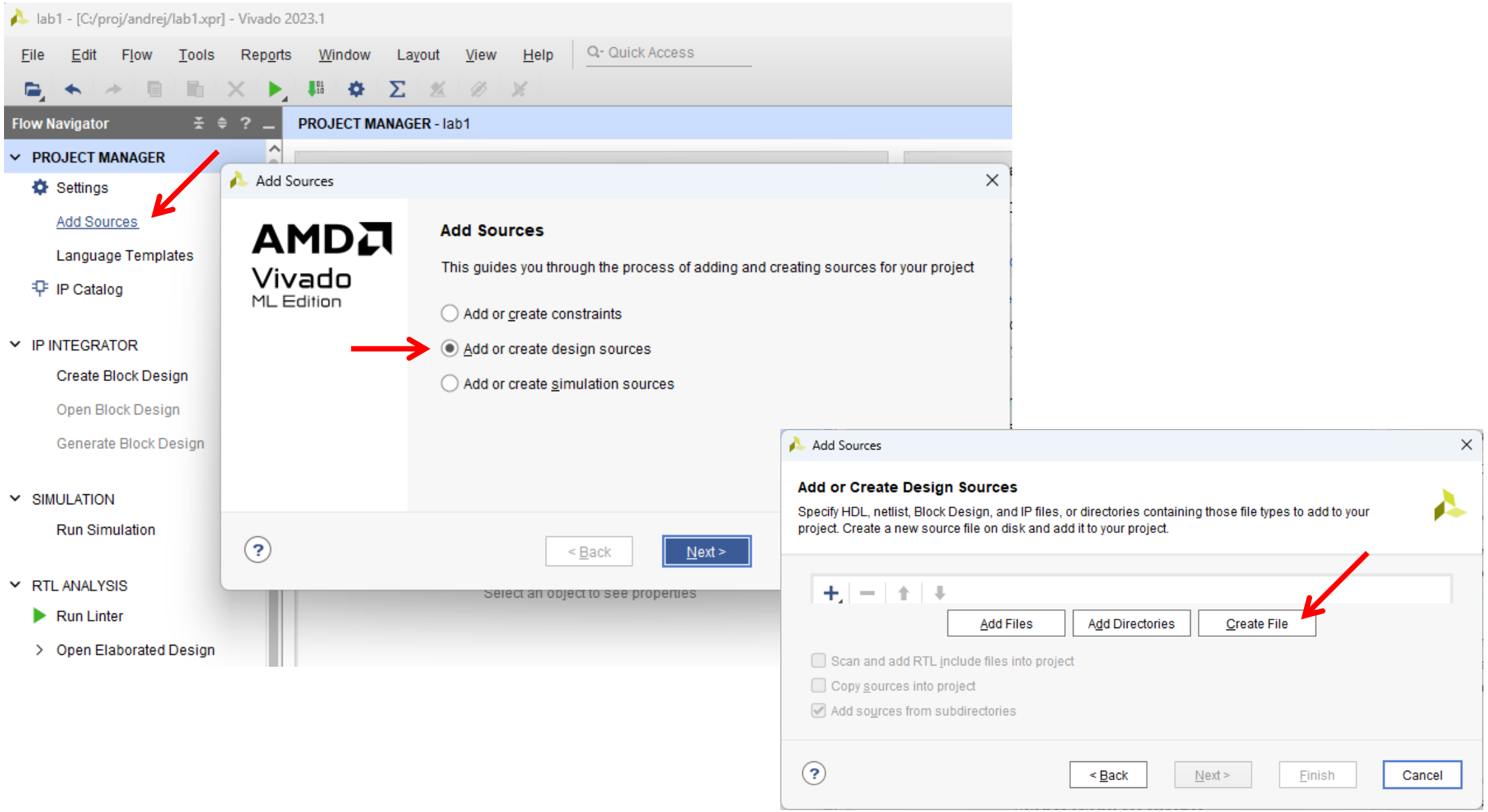



Vnesemo: ime projektne mape in lokacijo projekta (C:/proj/ime)

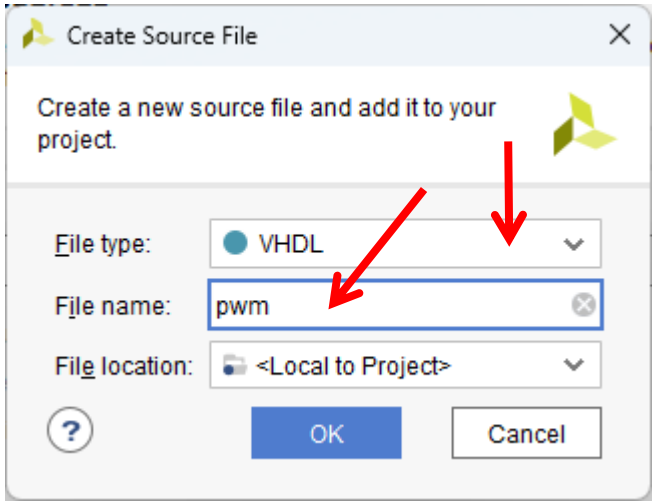
Preskočimo dodajanje datotek in zahtev…
Nastavimo: Default Part (Boards, avnet.com, MiniZed)

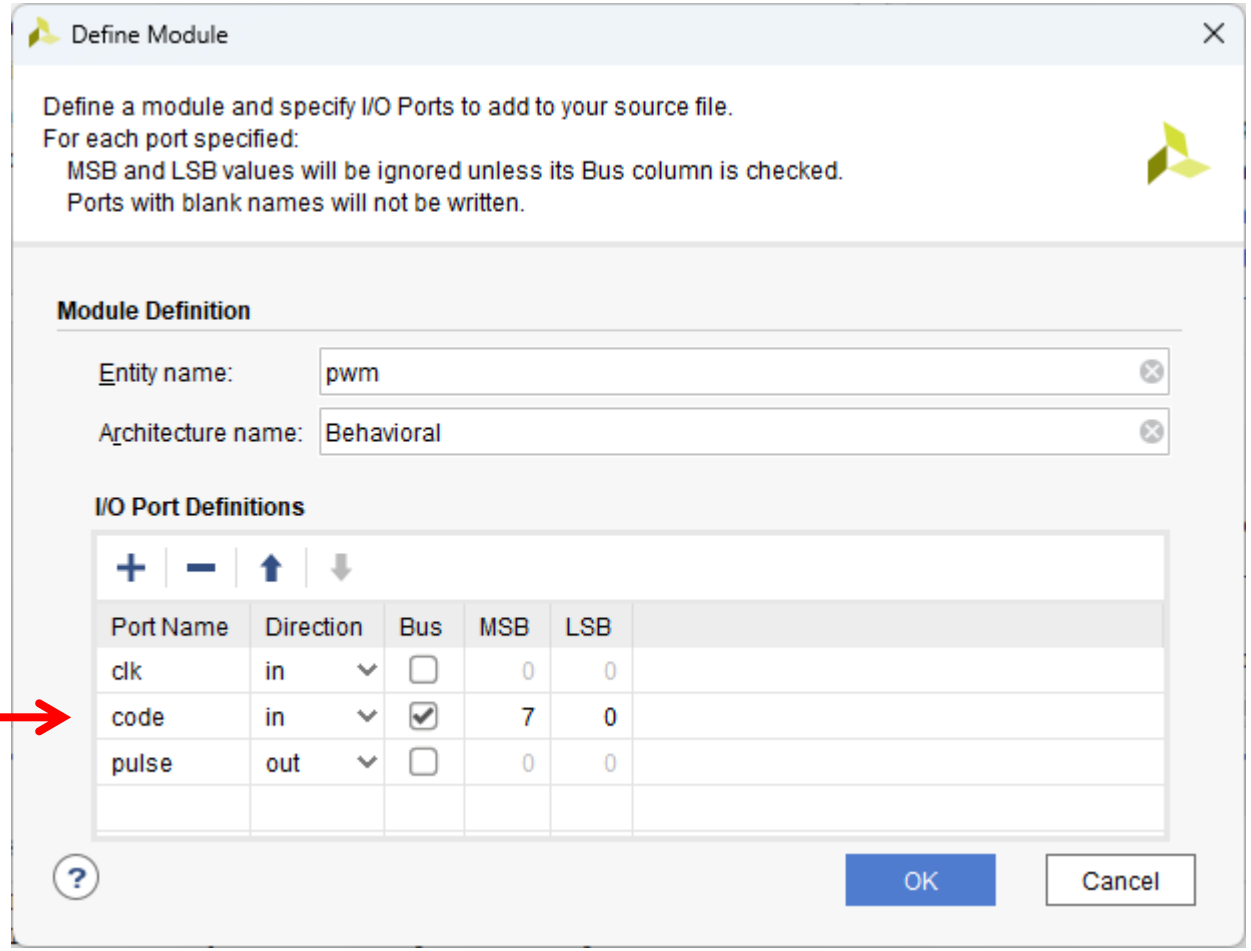


# Dodaj opis vezja (Add Sources, design sources)

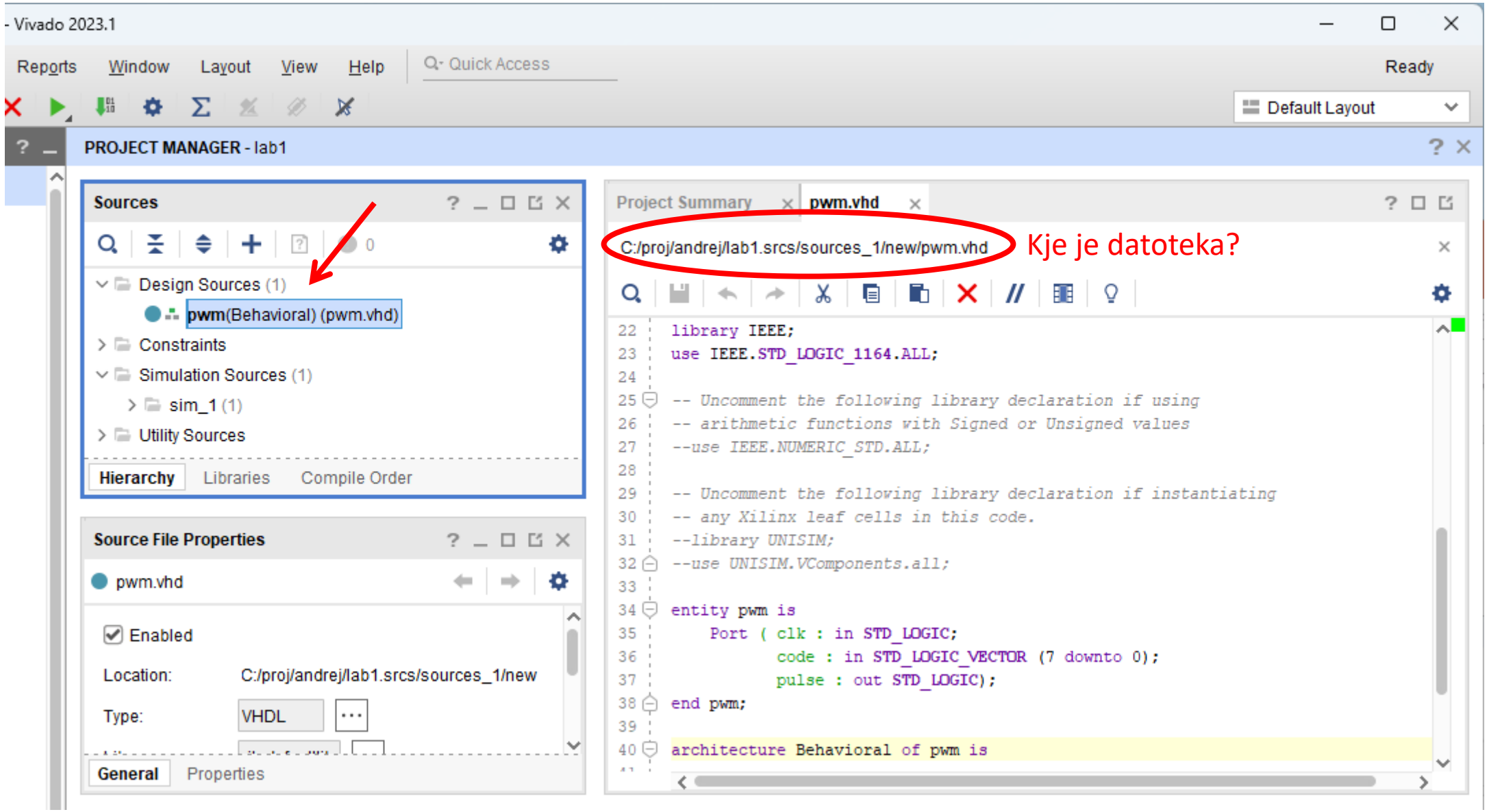


# VHDL model

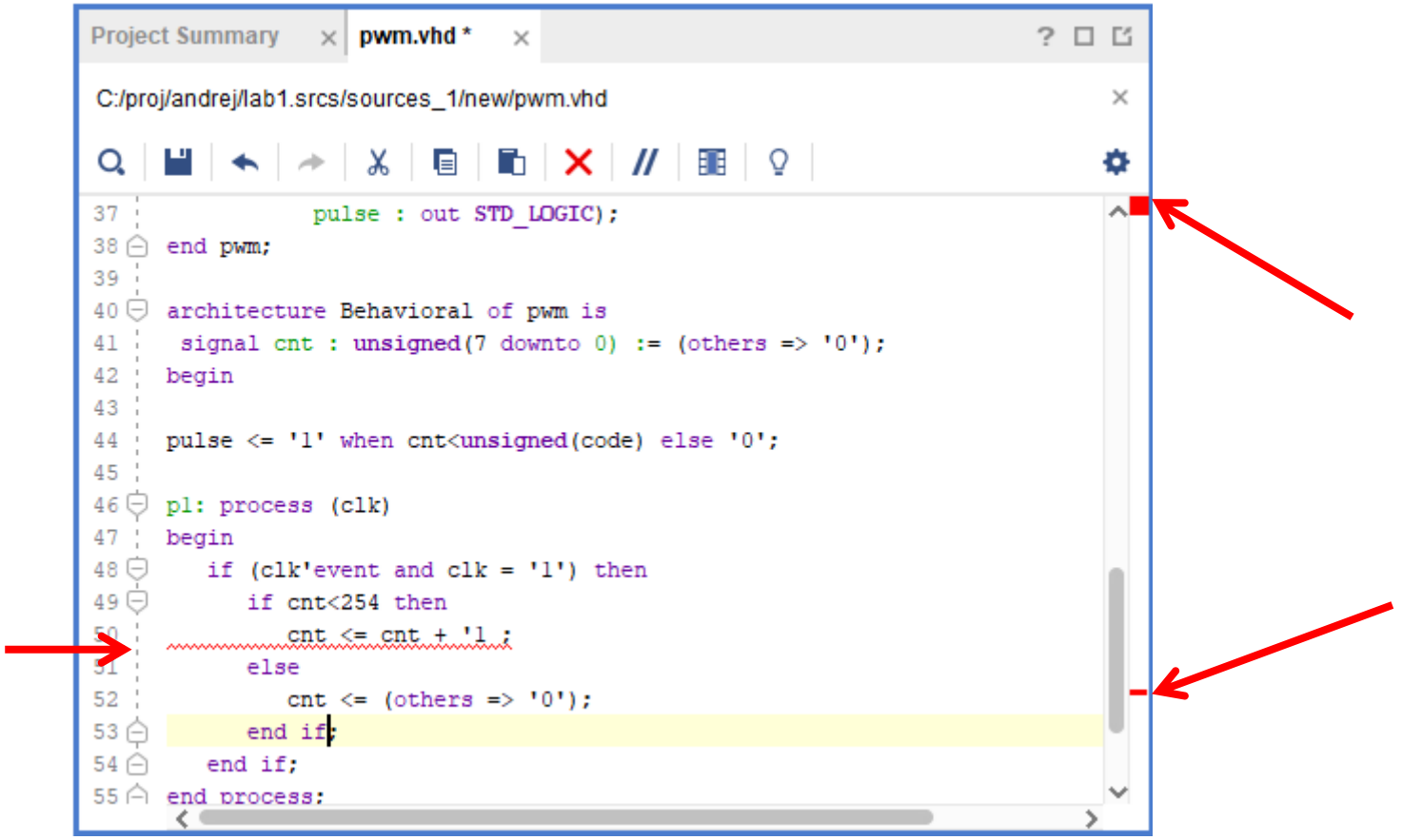

Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
pwm
File location:
<Local to Project>
OK
Cancel


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
pwm
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
clk
in
0
0
code
in
7
0
pulse
out
0
0
OK
Cancel

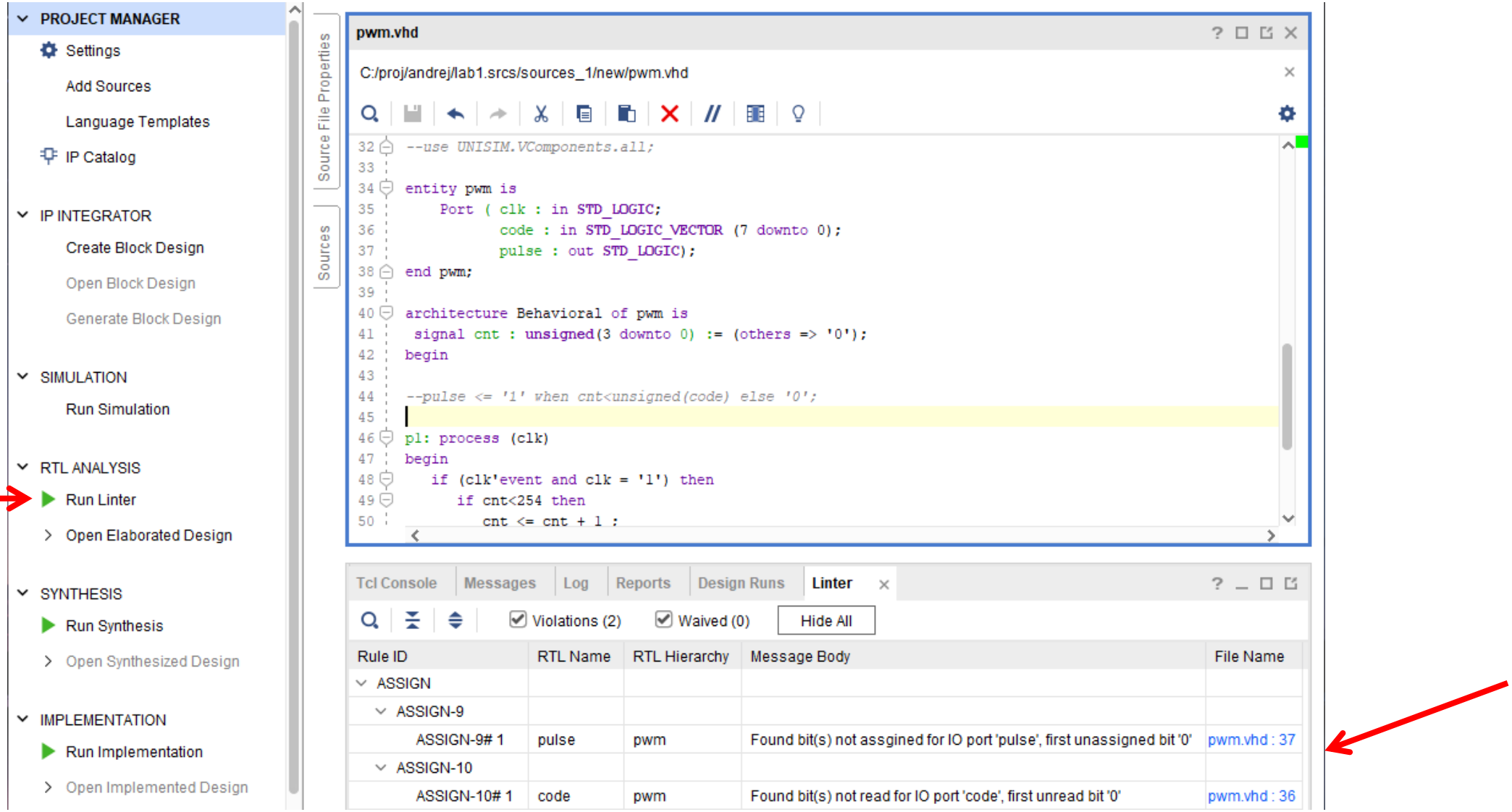
# Odpri izvorno kodo pwm.vhd



# Preverjanje sintakse med pisanjem kode



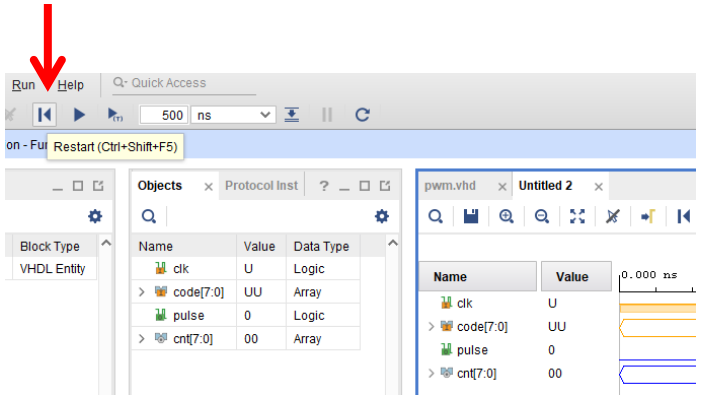
# Analiza kode: Linter

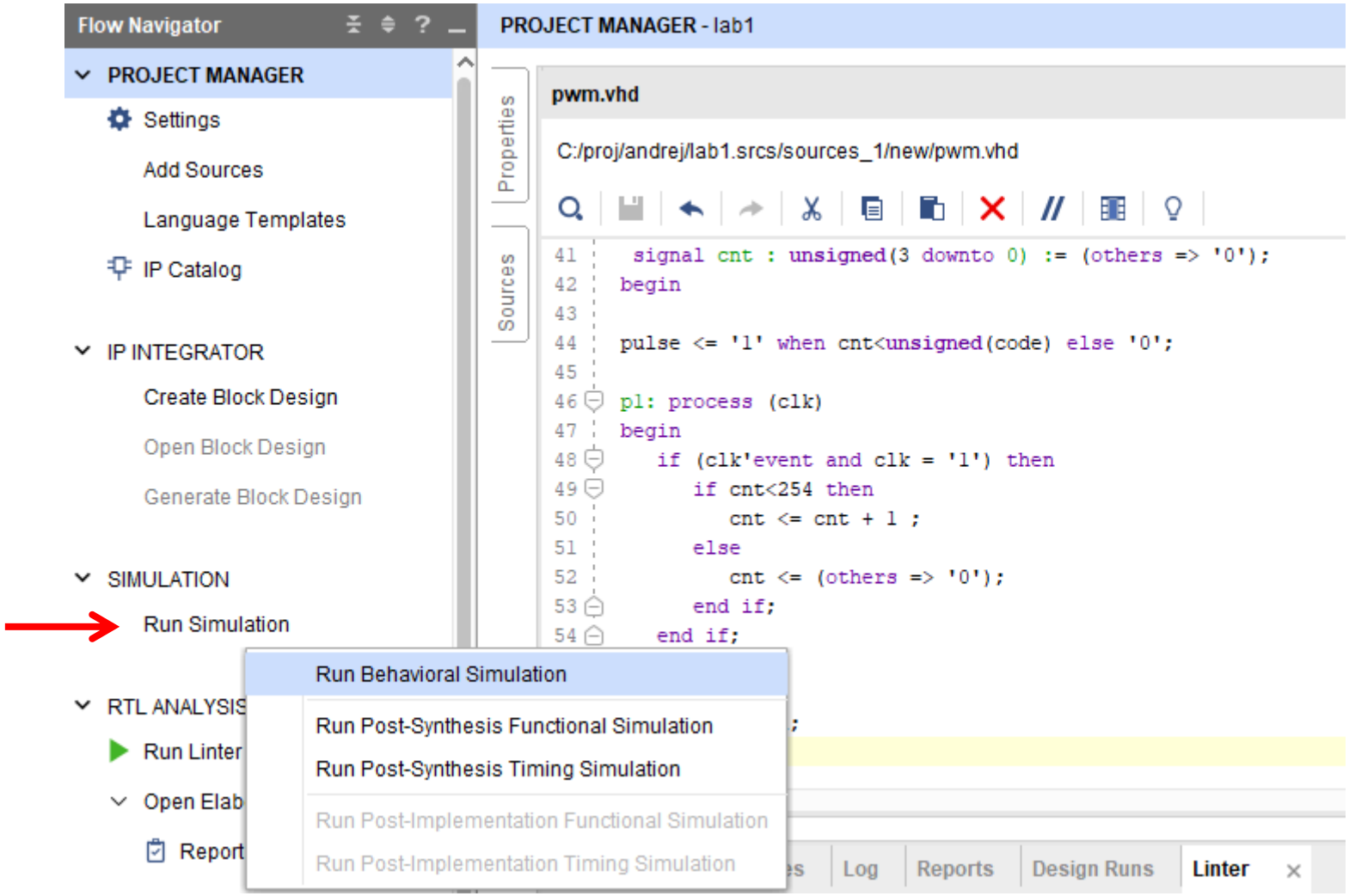


# Simulacija

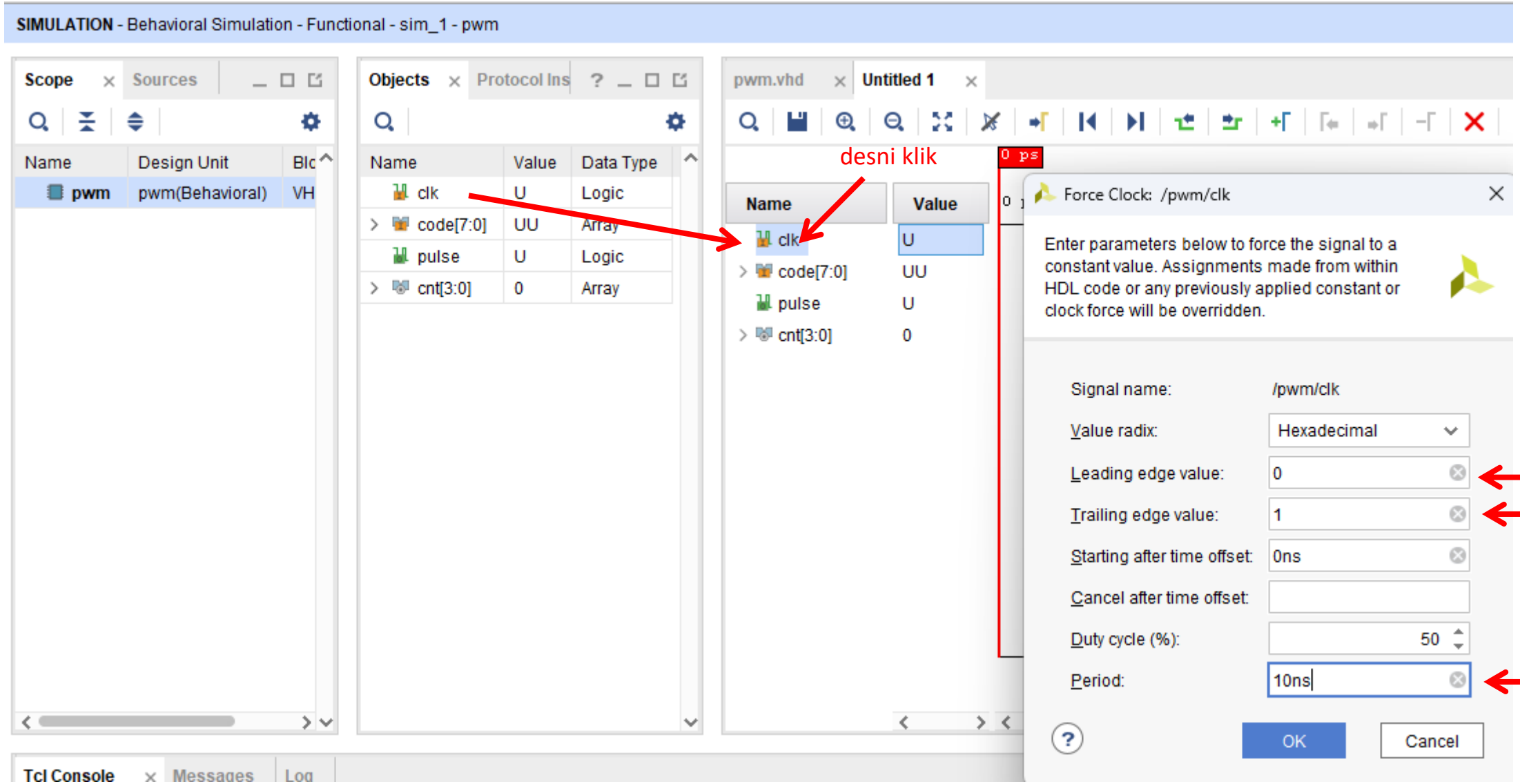
Simulacija se avtomatsko izvede.

Če ni testne strukture, naredimo Restart

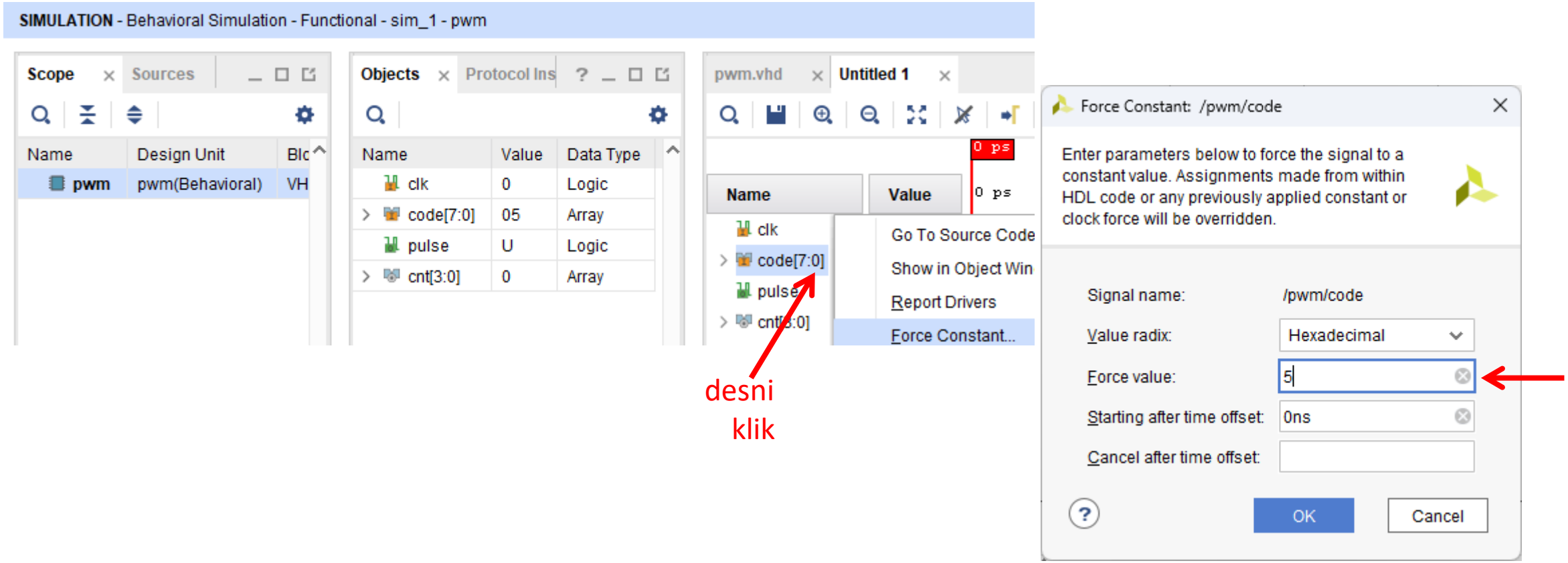


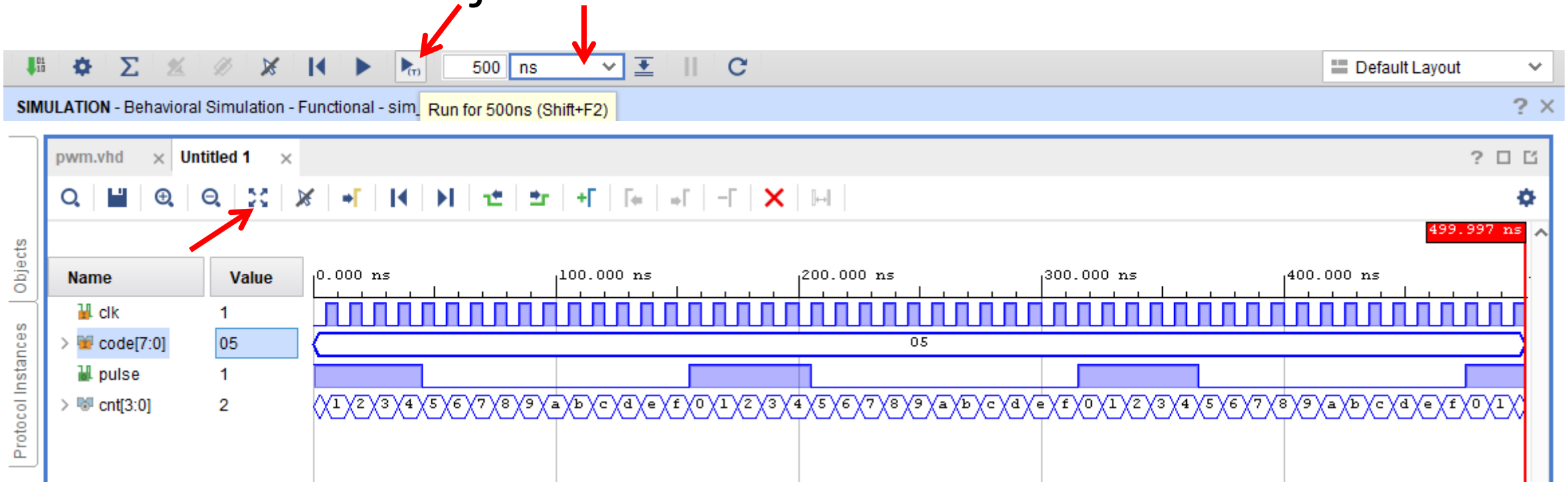
# Nastavi vhode: ura, Force Clock



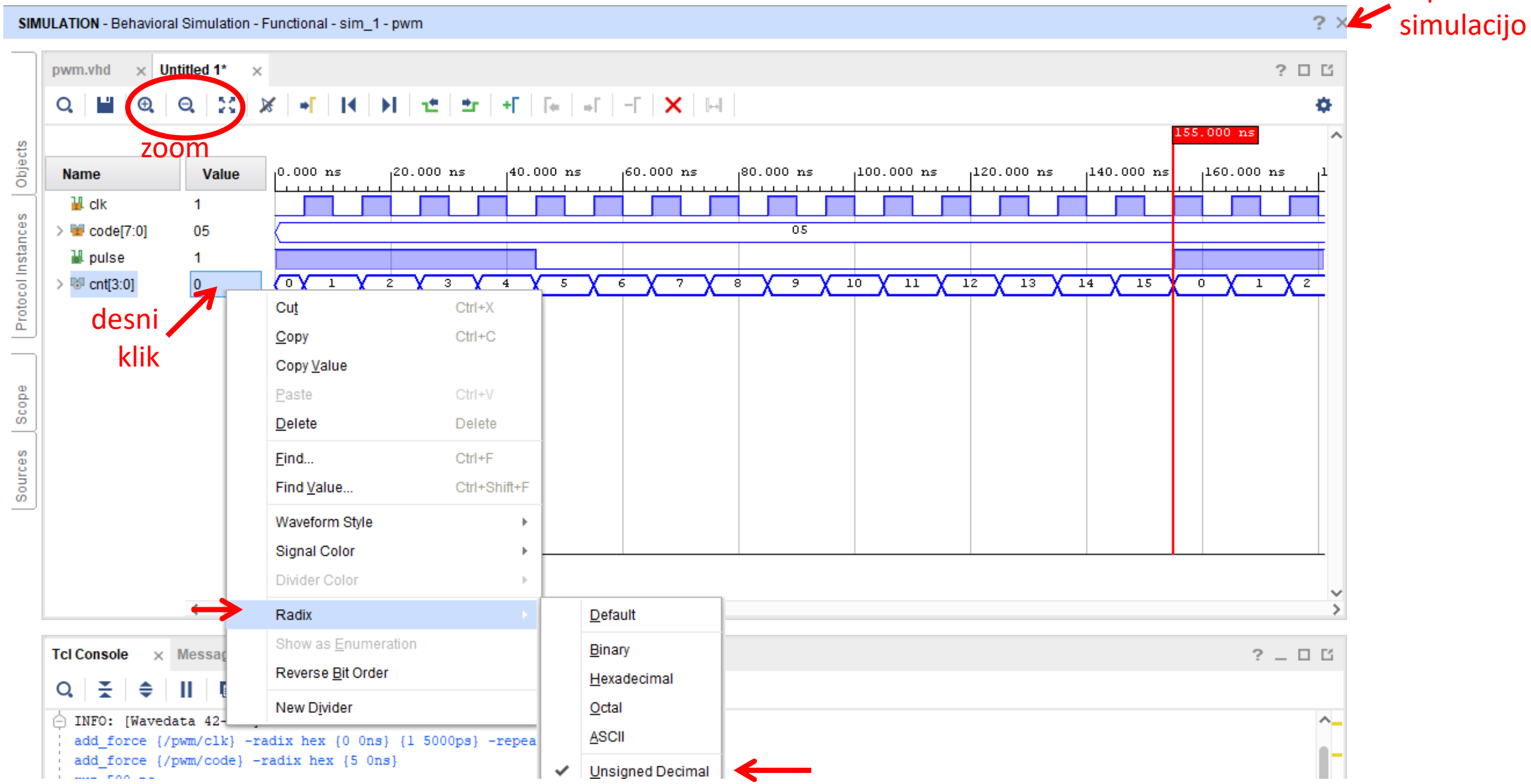
# Konstanten vhod



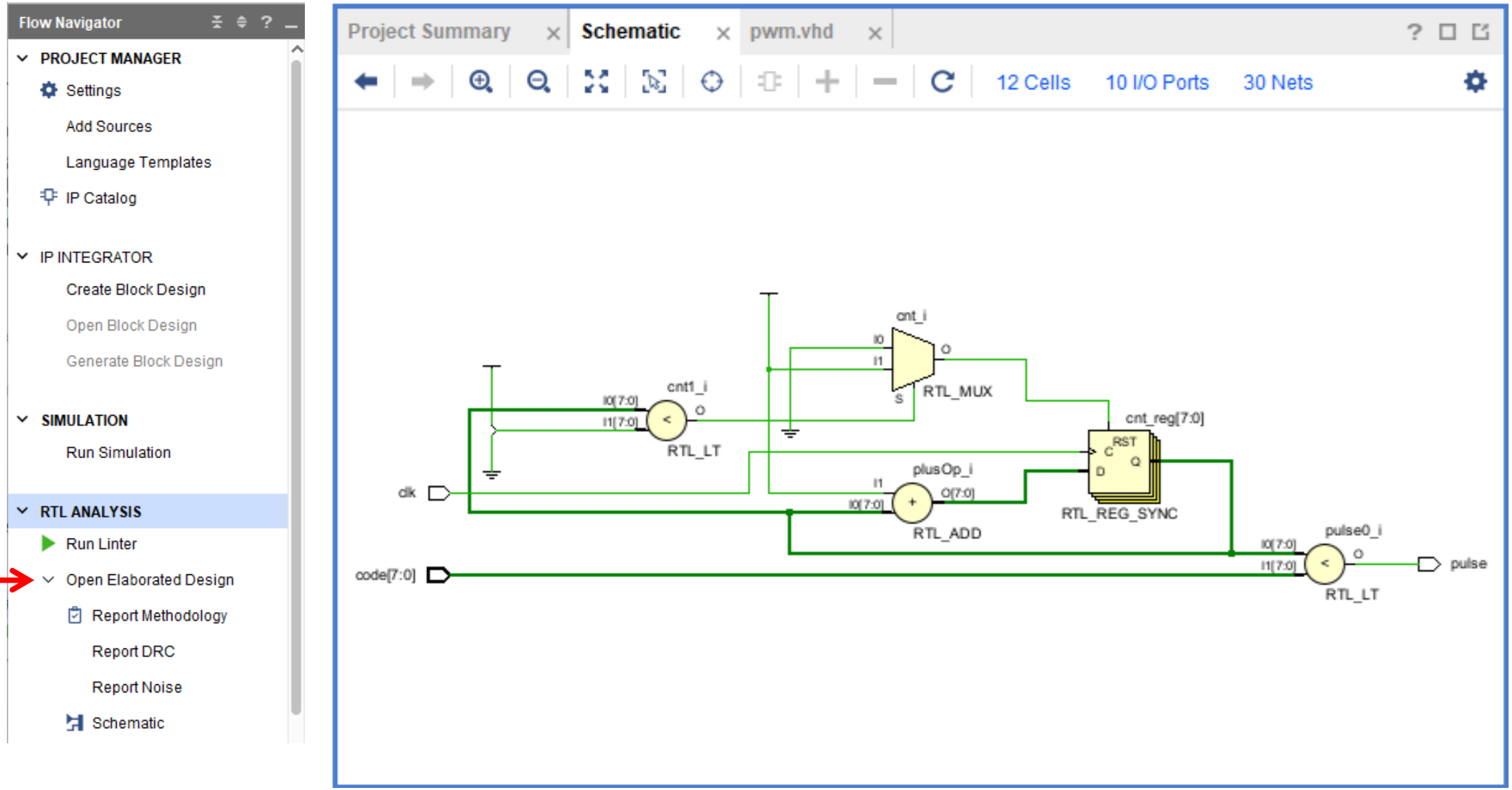
# Izvedi simulacijo



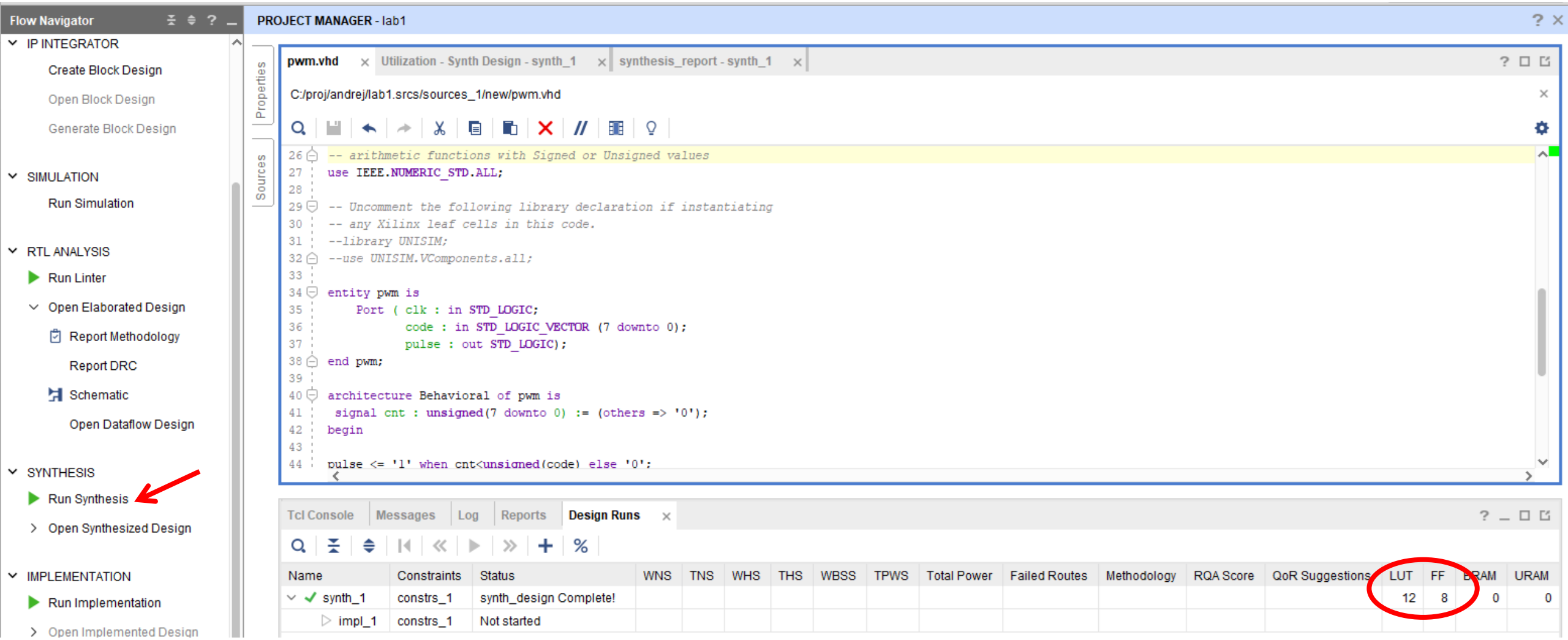
# Prikaz vrednosti (zoom, radix)



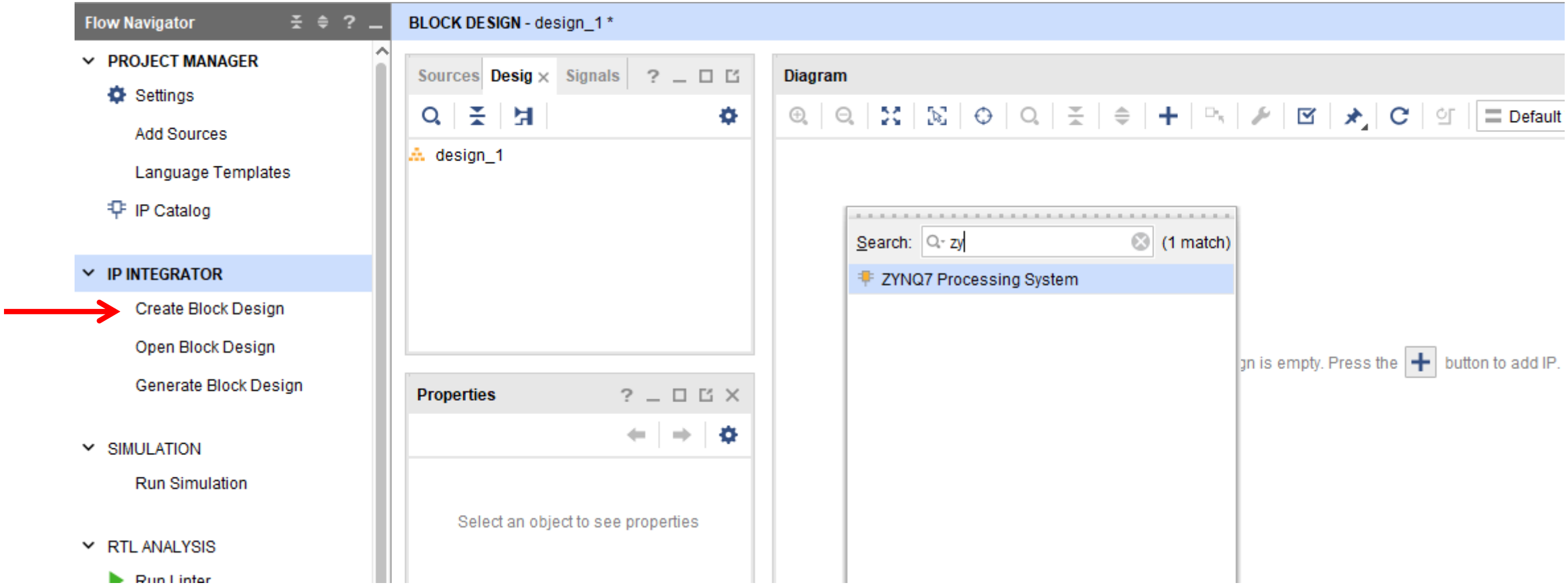
# RTL shema (Open Elaborated Design)



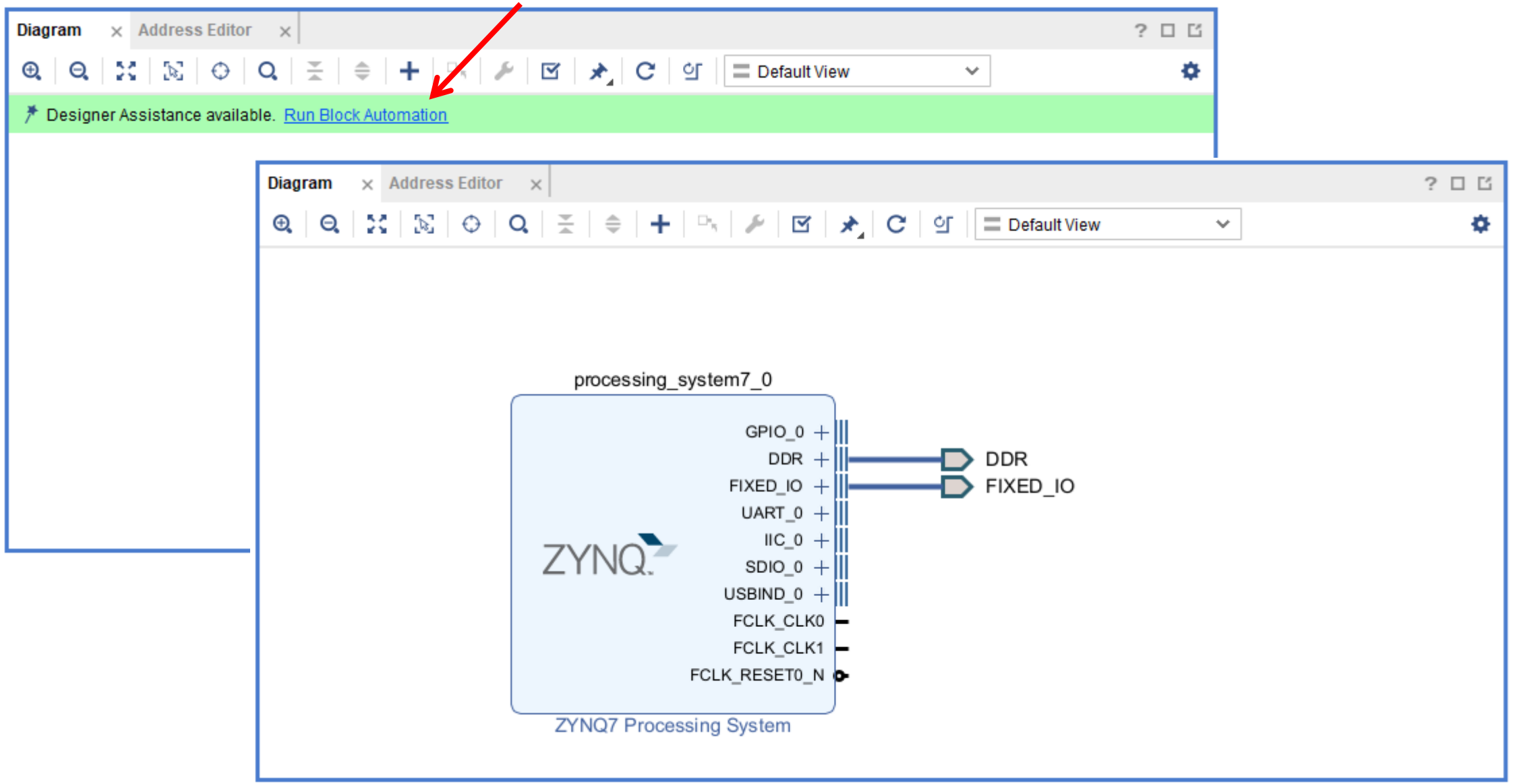
# Sinteza vezja: Flow > Run Synthesis > View Reports



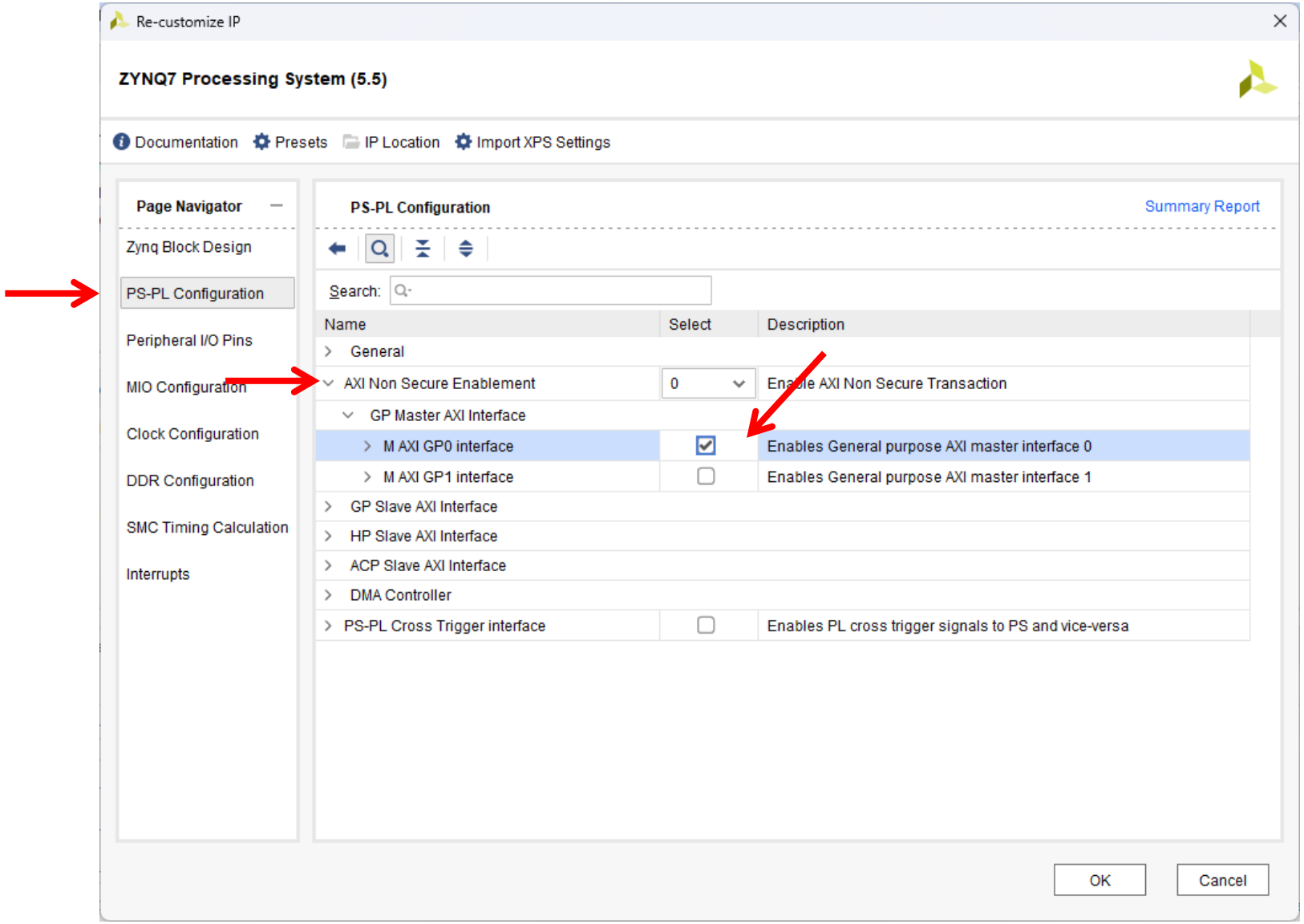
# Blokovni načrt s procesorjem



# Blokovni načrt s procesorjem

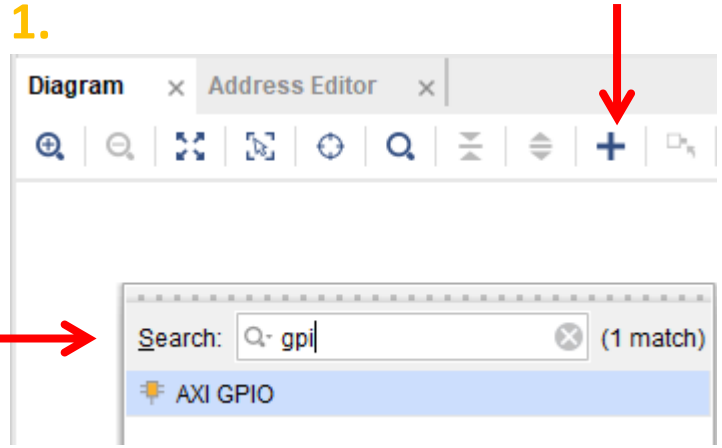


# Nastavi Zynq7

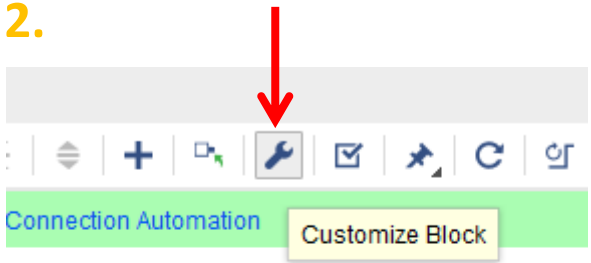


# Dodaj vmesnik GPIO z 8-bitnim izhodom

1.



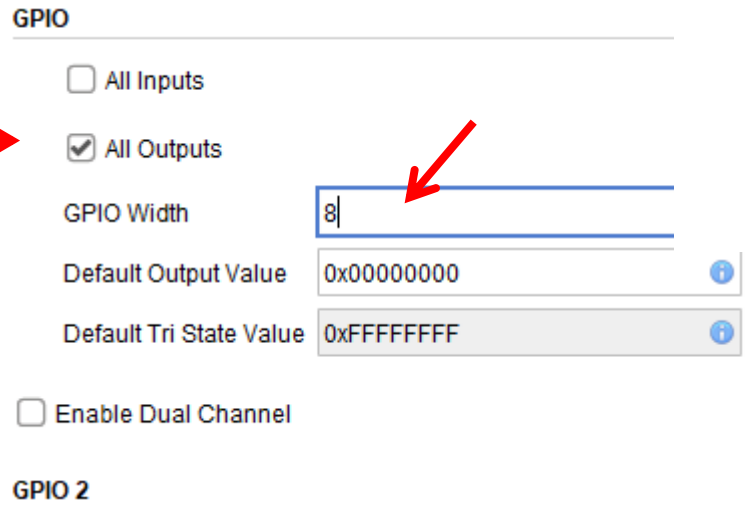

2.



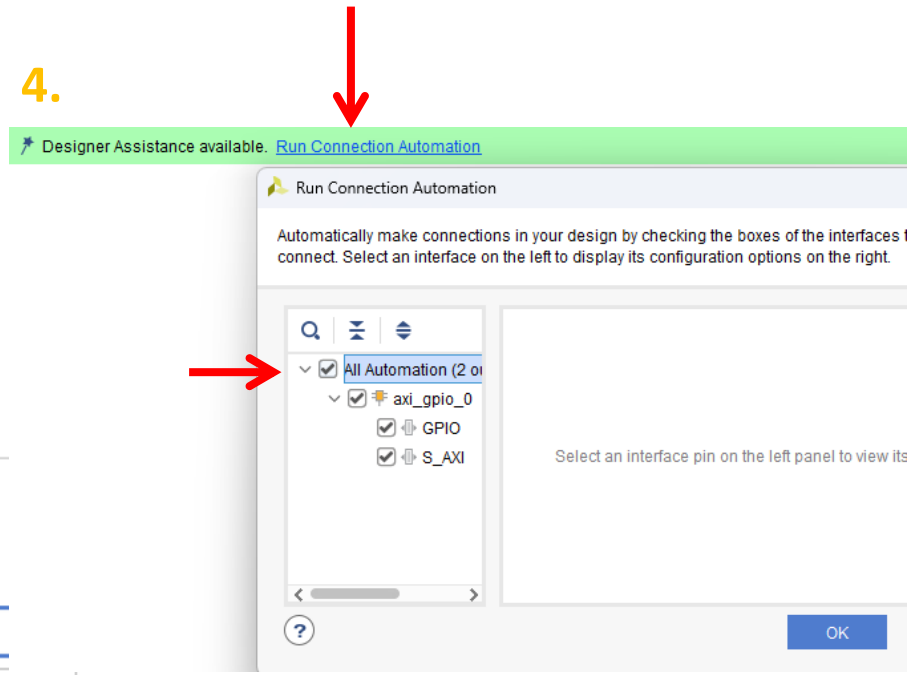

izberi


3.

nastavi




4.



# Zynq in GPIO

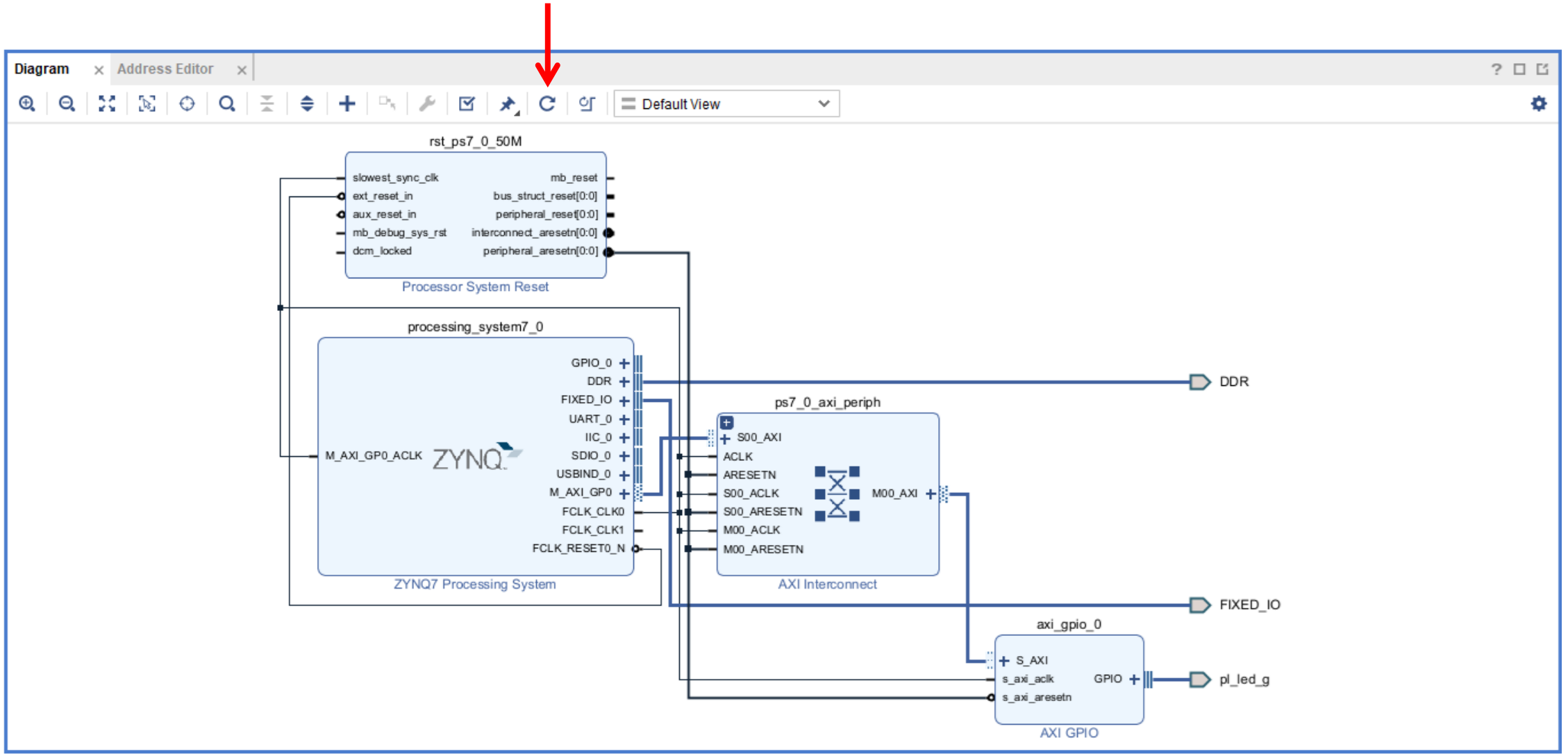
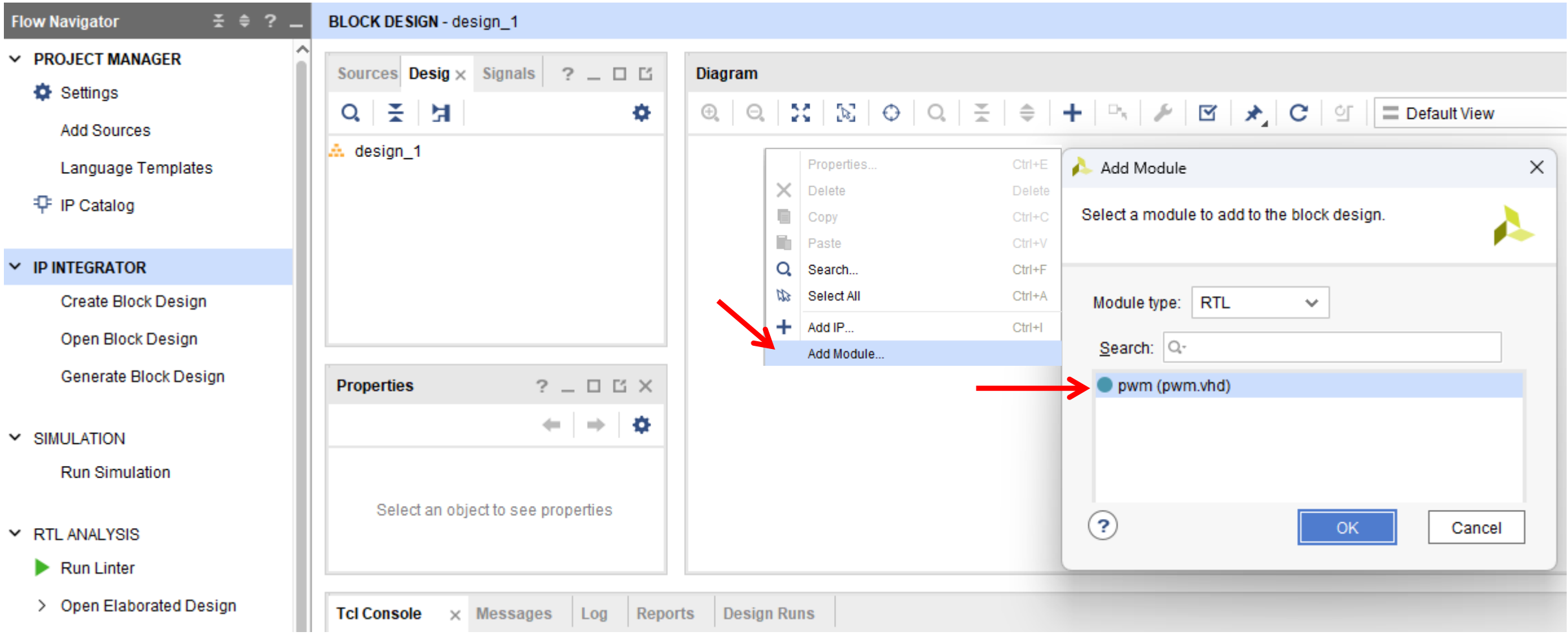
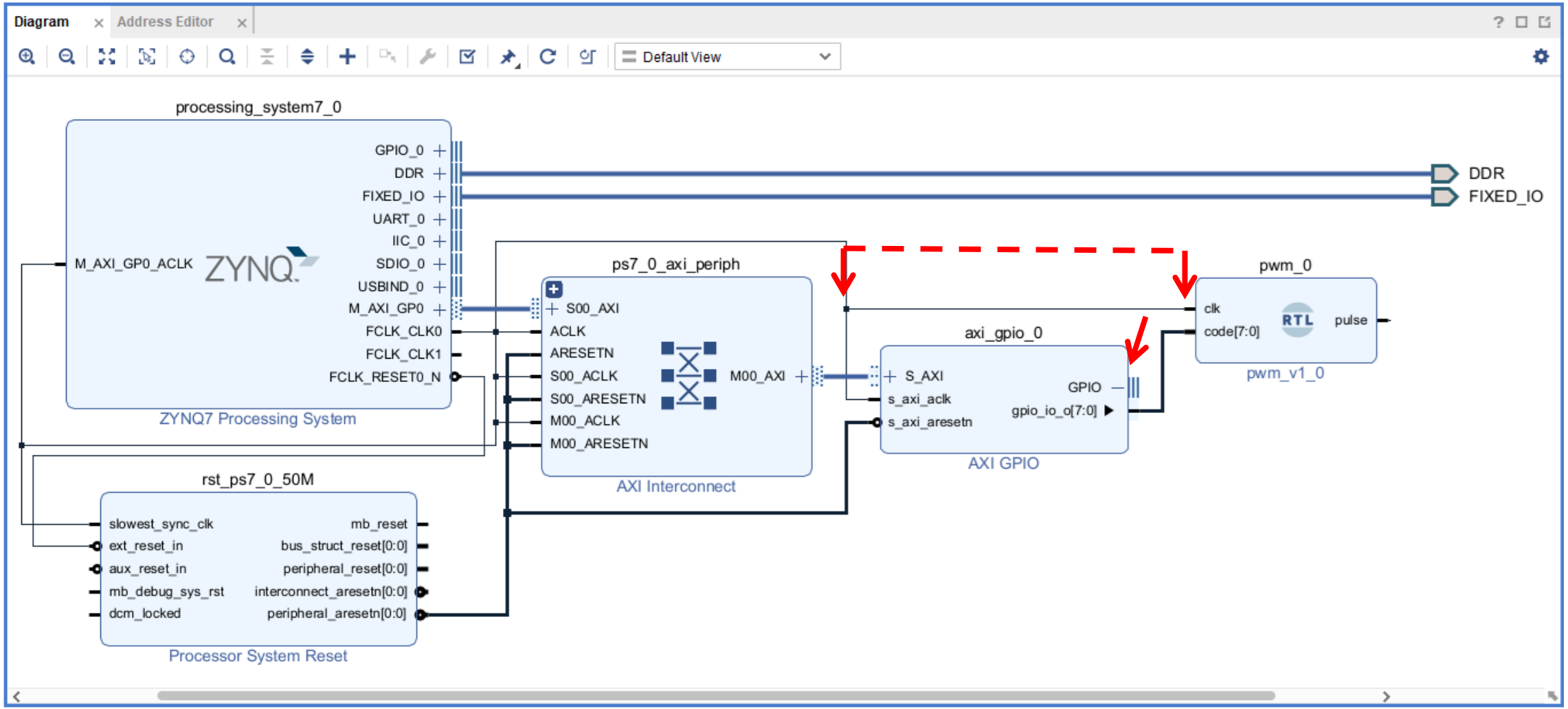


Diagram
Address Editor
Default View
rst_ps7_0_50M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
processing_system7_0
GPIO_0
DDR
FIXED_IO
UART_0
IIC_0
SDIO_0
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_CLK1
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ7 Processing System
ps7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
DDR
FIXED_IO
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
pl_led_g
AXI GPIO

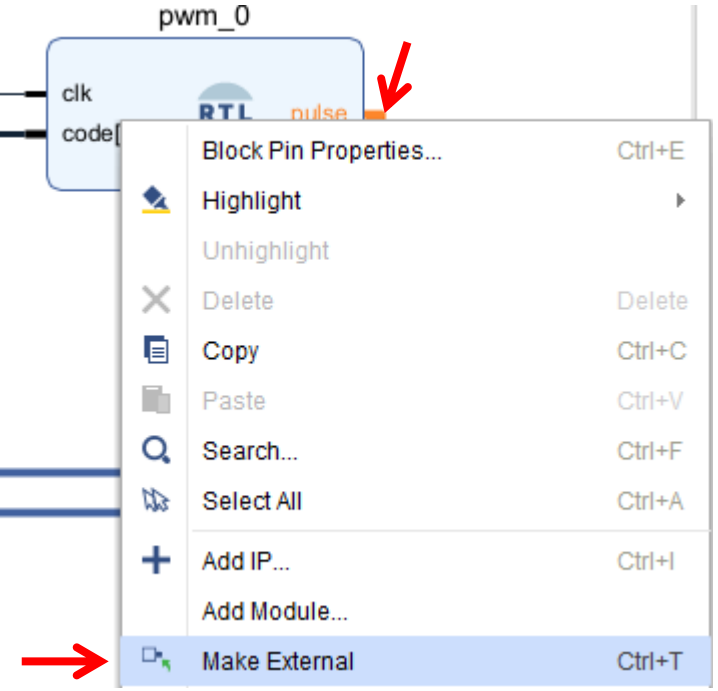
# Dodajaj VHDL komponento



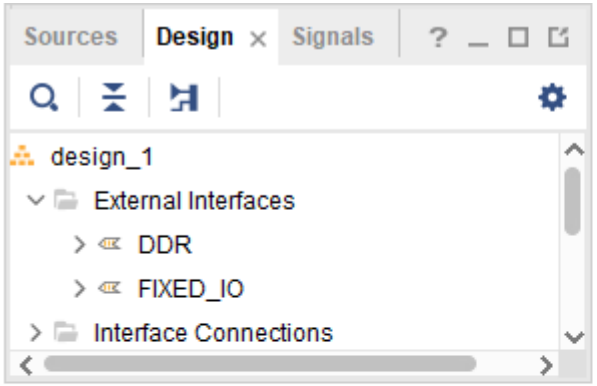
# Ročno poveži

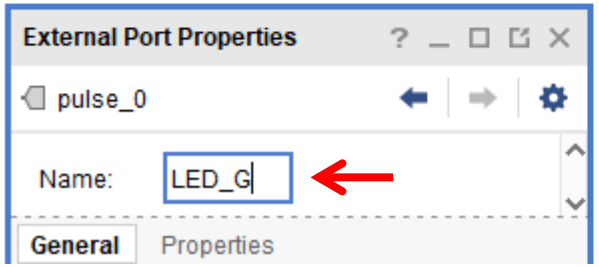


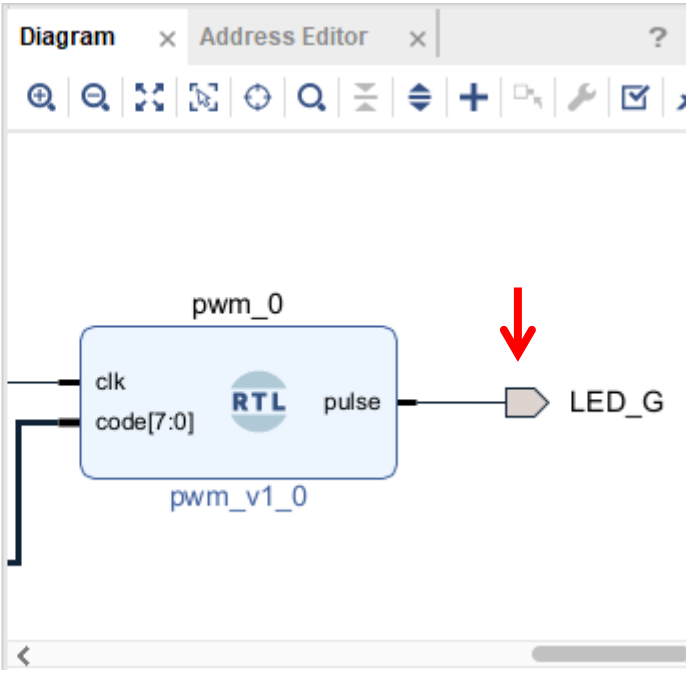
# Dodaj priključek



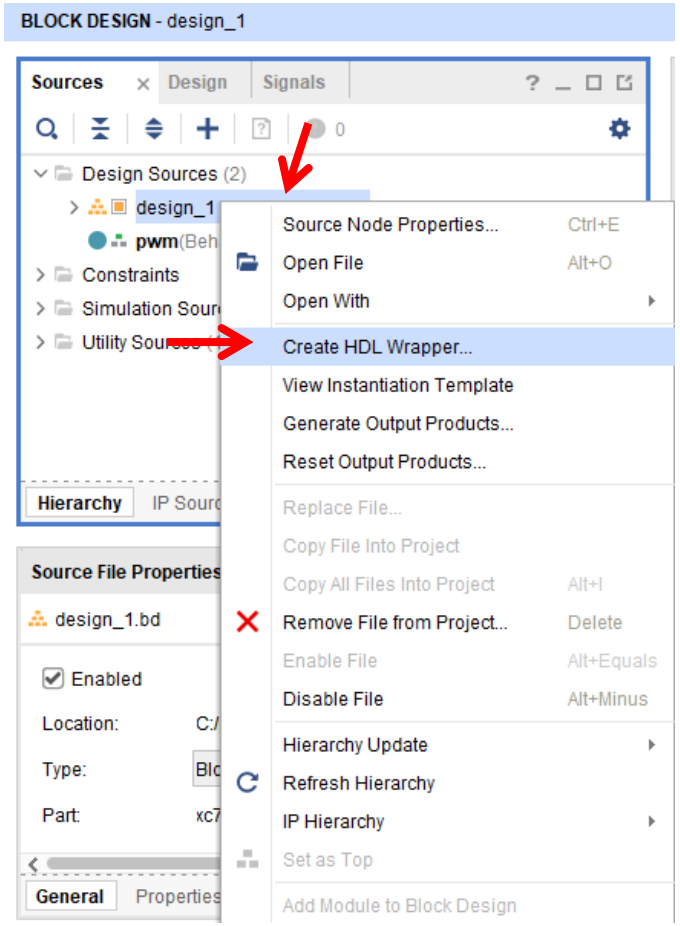

priključek pulse_0 preimenuj v LED_G

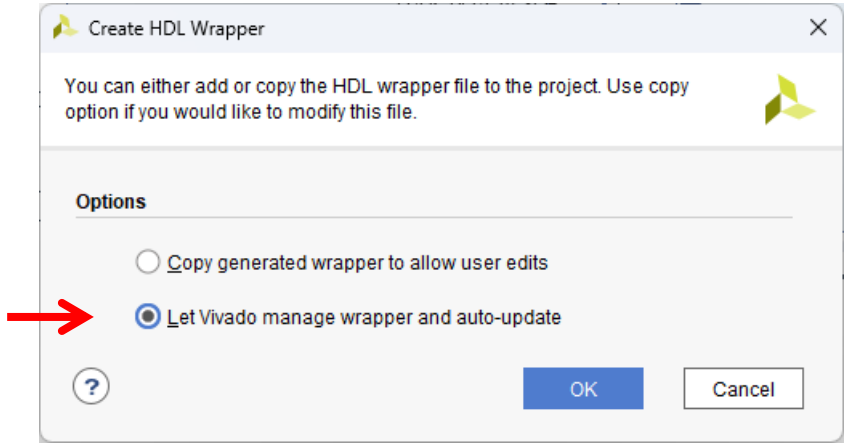


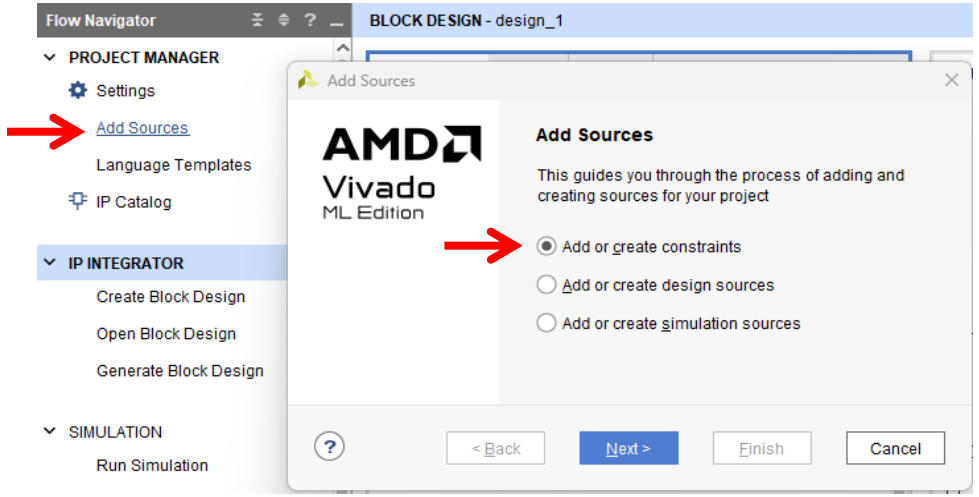



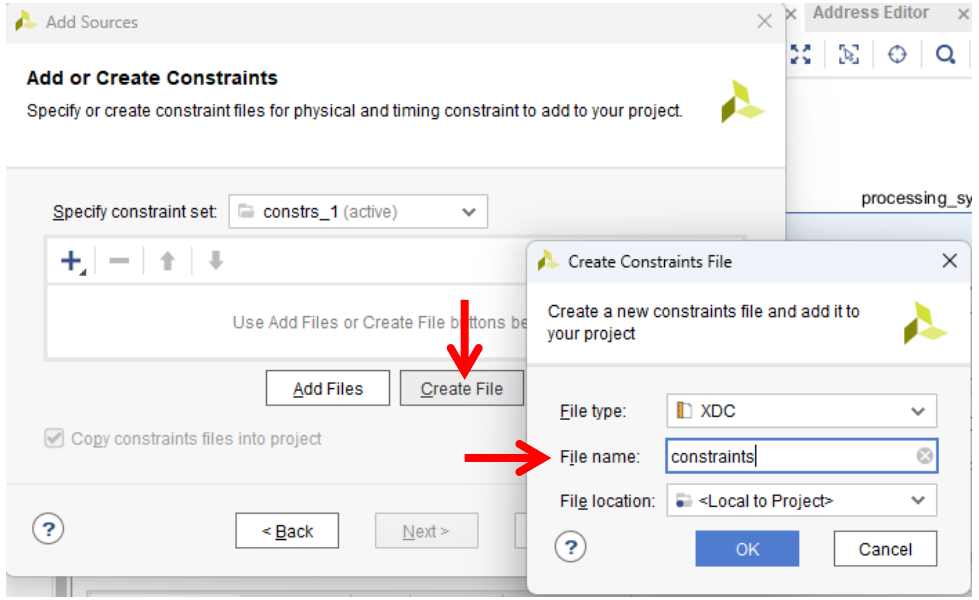
# Pretvori blokovni načrt v HDL

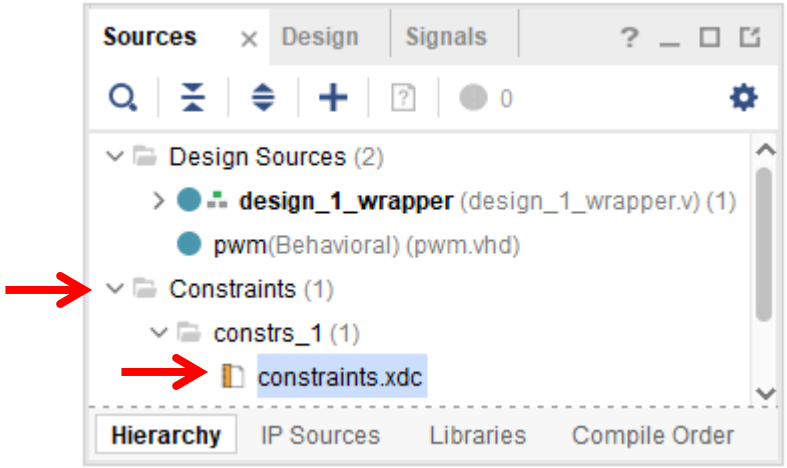


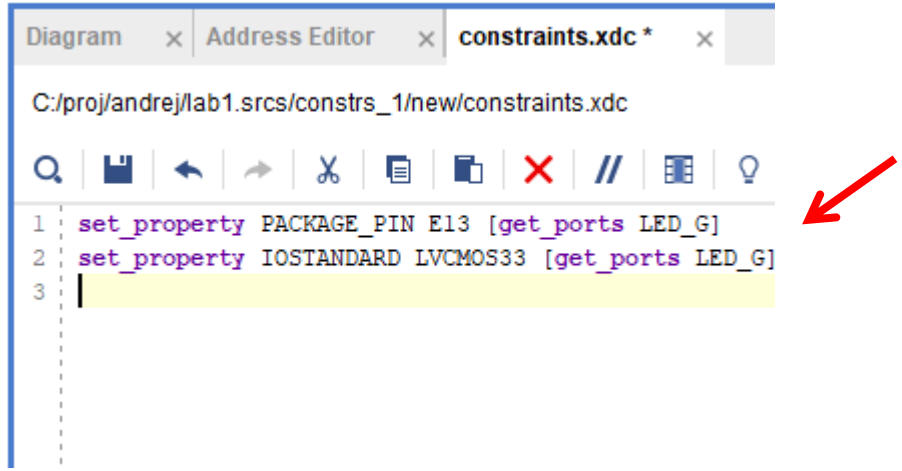



# Nastavitve priključkov

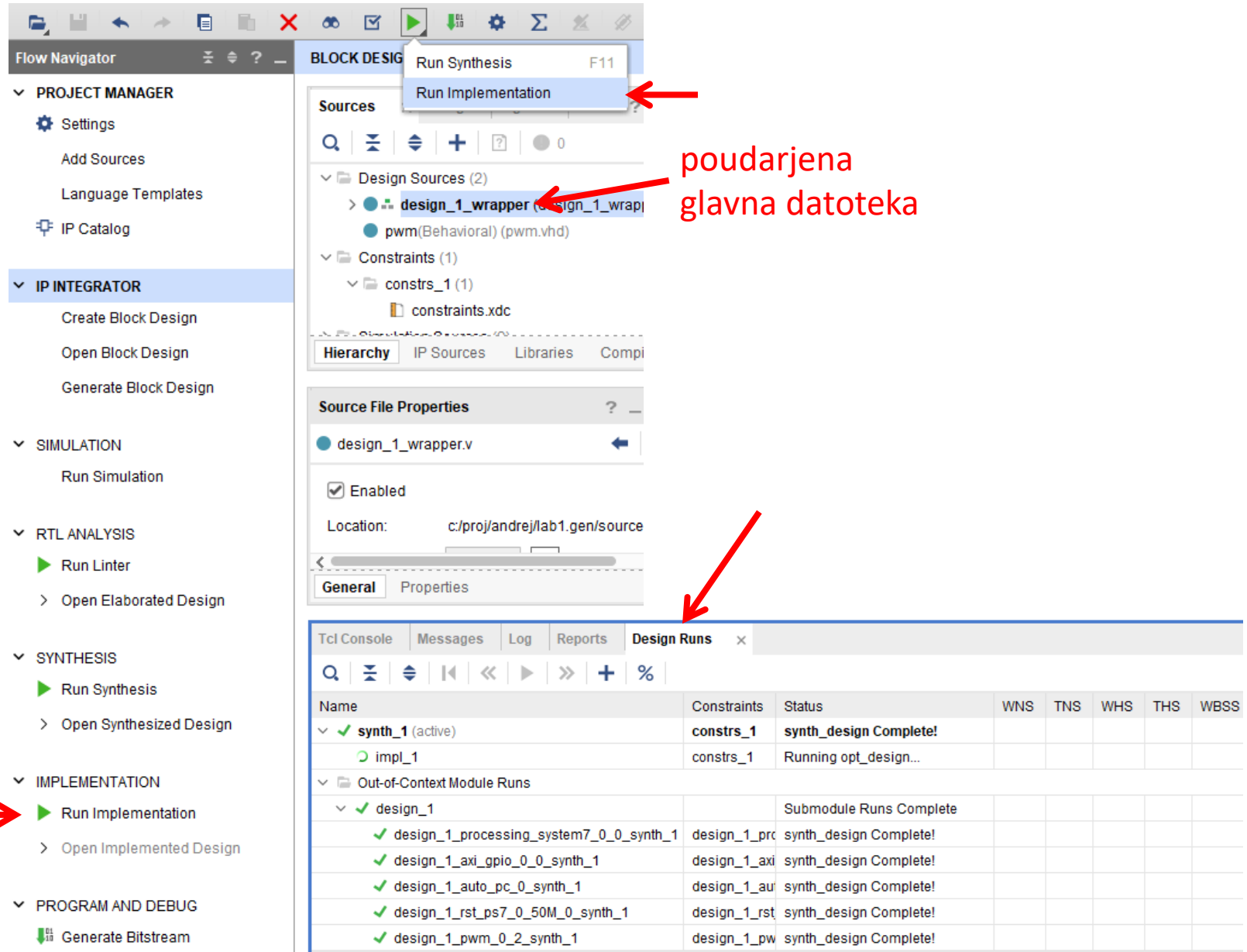


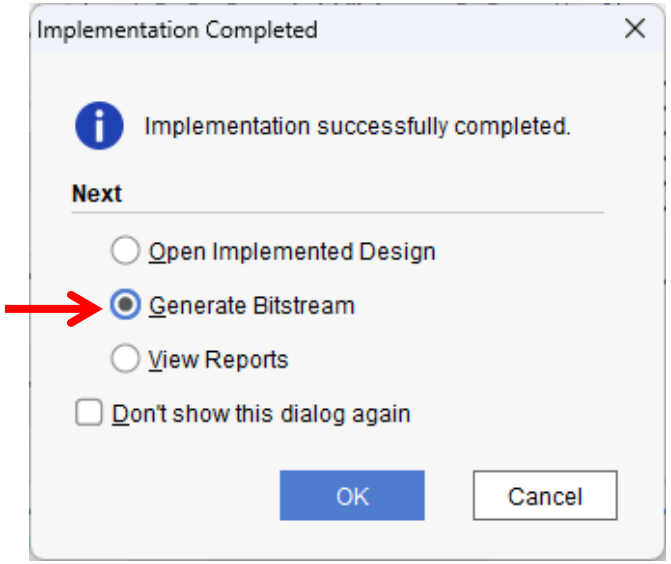



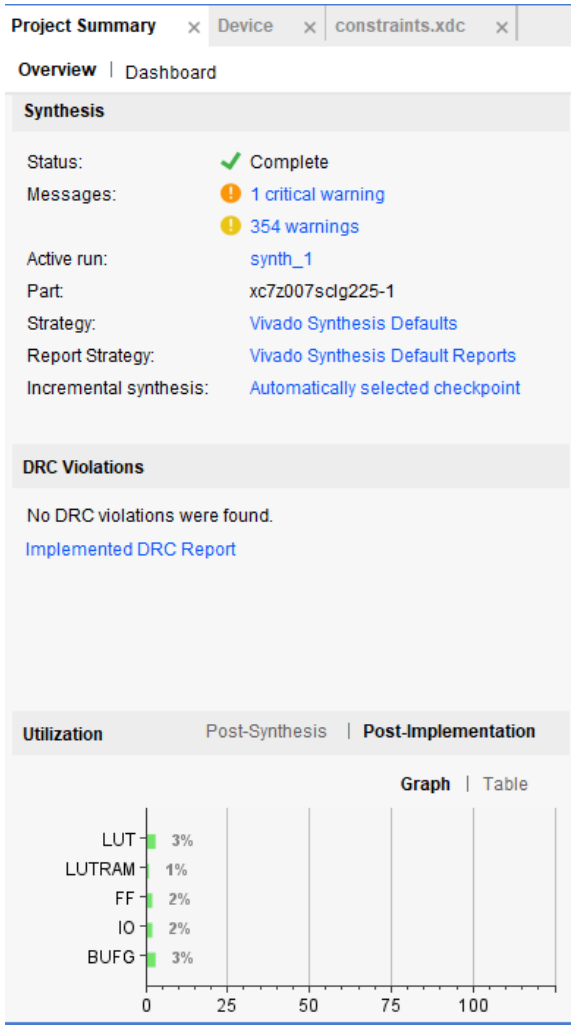
# Prevajanje: sinteza, implementacija

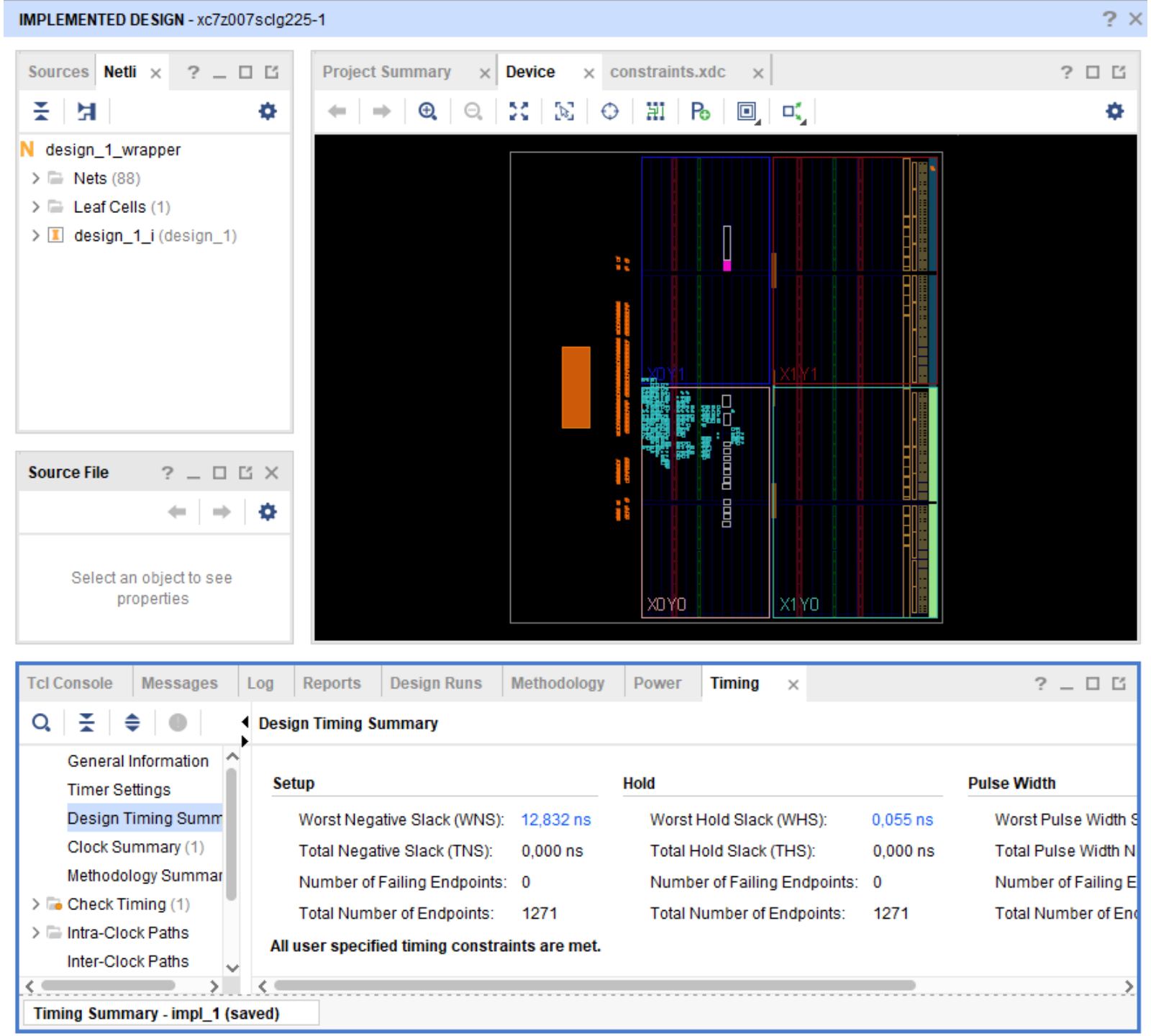



poudarjena
glavna datoteka

# Rezultat


Project Summary
Device
constraints.xdc
Overview | Dashboard
Synthesis
Status: Complete
Messages: 1 critical warning
354 warnings
Active run: synth_1
Part: xc7z007sclg225-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: Automatically selected checkpoint
DRC Violations
No DRC violations were found.
Implemented DRC Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 3%
LUTRAM 1%
FF 2%
IO 2%
BUFG 3%
0
25
50
75
100


IMPLEMENTED DESIGN - xc7z007sclg225-1
Sources
Netli
design_1_wrapper
Nets (88)
Leaf Cells (1)
design_1_i (design_1)
Source File
Select an object to see properties
Project Summary
Device
constraints.xdc
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Methodology
Power
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summ
Clock Summary (1)
Methodology Summar
Check Timing (1)
Intra-Clock Paths
Inter-Clock Paths
Setup
Worst Negative Slack (WNS): 12,832 ns
Total Negative Slack (TNS): 0,000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1271
Hold
Worst Hold Slack (WHS): 0,055 ns
Total Hold Slack (THS): 0,000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1271
Pulse Width
Worst Pulse Width S
Total Pulse Width N
Number of Failing E
Total Number of End
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)