

# Sistem na čipu Zynq in Vivado

[Vivado](#), [VHDL model](#), [simulacija](#), [sinteza](#)  
[blokovni načrt](#), [priključki](#), [prevajanje](#)

Andrej Trost

Laboratorij za načrtovanje integriranih vezij



UNIVERZA  
V LJUBLJANI

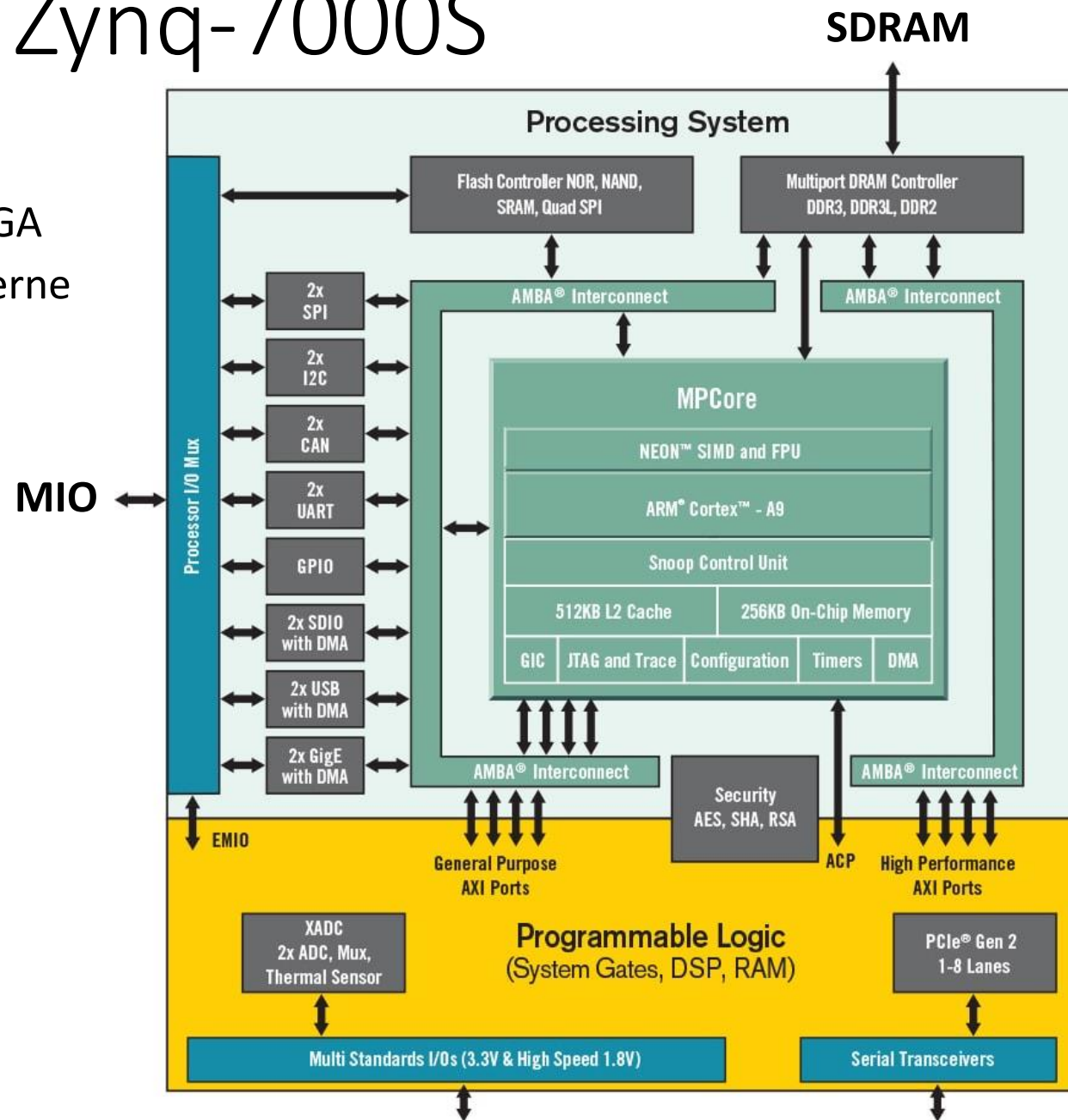
**FE**

Fakulteta  
za elektrotehniko

# AMD-Xilinx Zynq-7000S

## ► Sistem na čipu (SoC)

- ARM Cortex-A9 in FPGA
- multipleksirane periferne enote (MIO)
- na FPGA povezani vmesniki AXI



# Razvojne plošče

MiniZed

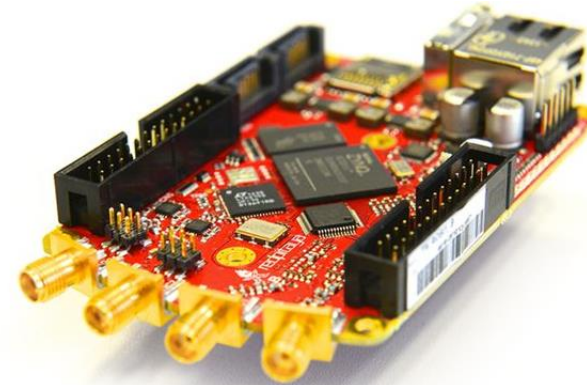


- ▶ **XC7Z007S**  
Artix-7 + ARM Cortex-A9  
14k LUT / 29k FF  
66 DSP48  
50 BRAM (36k)  
XADC
- ▶ DDR3, Flash, eMMC
- ▶ USB, Wi-Fi, BLE
- ▶ senzor gibanja, temp  
mikrofon

Cora Z7-07S



Red Pitaya



- ▶ **XC7Z010**  
2xARM Cortex-A9  
17k LUT / 35k FF  
80 DSP48  
60 BRAM
- ▶ AD/DA 125 Msps
- ▶ Linux

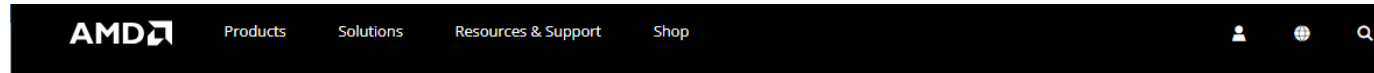
ZedBoard



- ▶ **XC7Z020**  
2xARM Cortex-A9  
53k LUT / 106k FF  
220 DSP48  
140 BRAM

# Namestitev Vivado 2023.1

<https://www.xilinx.com/support/download.html>



Adaptive Computing Support / Downloads

## Downloads

Licensing Help

NIC Software & Drivers

Vivado (HW Developer)

Vitis (SW Developer)

Vitis Embedded Platforms

Power Design Manager

Alveo Packages

PetaLinux

Device Models

Documentation Navigator

## Version

2024.1

2023.2

2023.1

Vivado Archive

ISE Archive

CAE Vendor Libraries Archive

### Vivado ML Edition - 2023.1 Full Product Installation

#### Important Information

Vivado™ ML 2023.1 is now available for download:

- Average QoR Improvement of 8% for Versal™ Adaptive SoCs and 13% for UltraScale+ FPGAs using Intelligent Design Runs
- Extending multithreading support for bitstream generation for Versal devices
- Enhancements in Report QoR Assessment (RQA)
- Power Design Manager (PDM) now a part of Unified Installer – Separate from Vivado tool
- Added support for Versal HBM devices in Power Design Manager (PDM)

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Installer Information](#) for details.

Download Includes

Vivado ML Edition

Download Type

Full Product Installation

Last Updated

May 17, 2023

Answers

[2023.x - Vivado Known Issues](#)

Documentation

[Release Notes](#)  
[OS Support Update](#)  
[What's New in Vivado](#)

Support Forums

[Installation and Licensing](#)

AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1: Windows Self Extracting Web Installer (EXE - 199.47 MB)

MD5 SUM Value : 4c6a1e5d5cf7c44c3f201c9056b6cf45

Download Verification

Digests

Signature

Public Key

## Select Product: o Vitis

AMD Unified Installer for FPGAs & Adaptive SoCs 2023.1 - Vitis Unified Software Platform

Vitis Unified Software Platform

Customize your installation by (de)selecting items in the tree below. Moving...

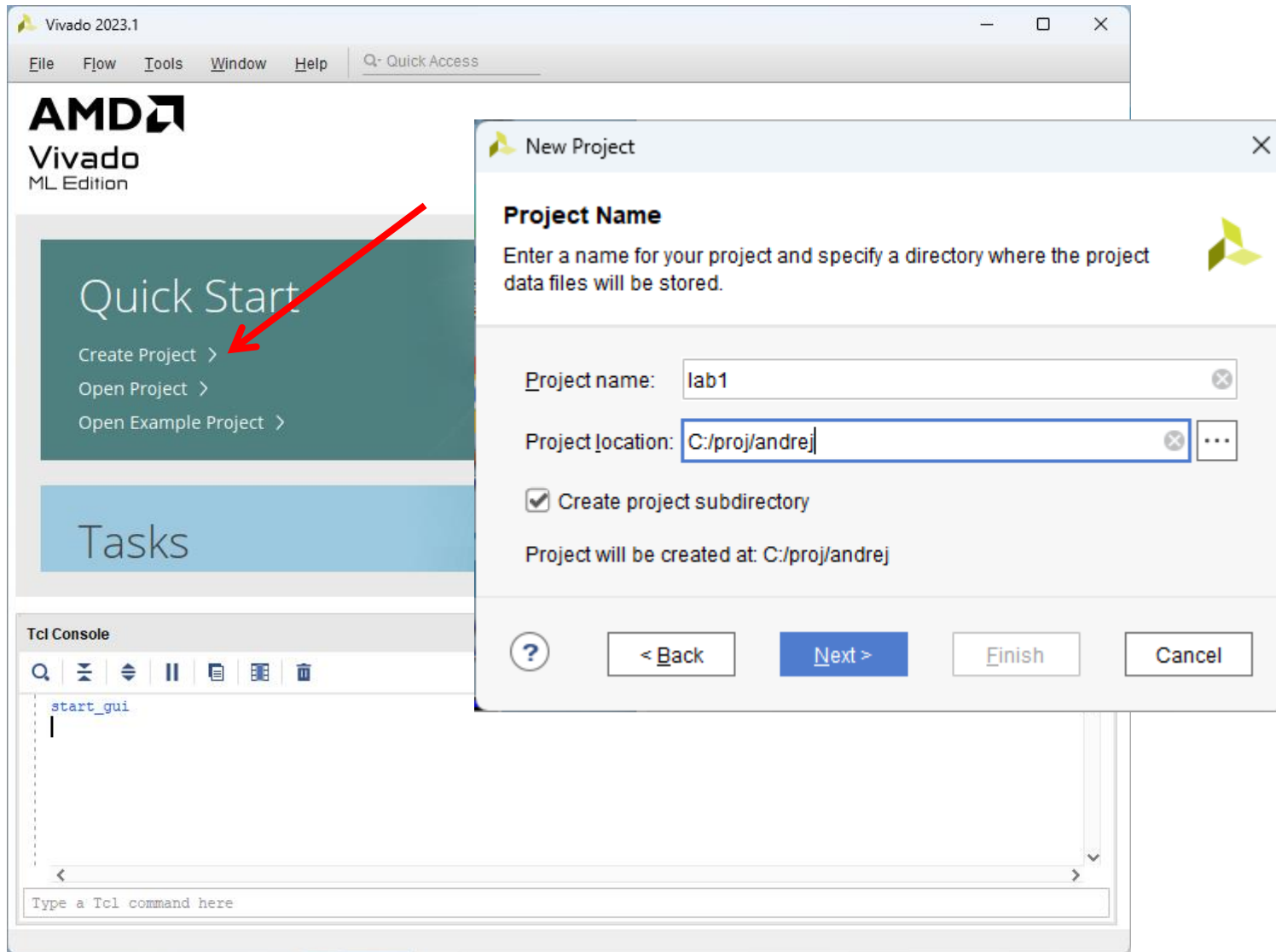
The Vitis unified software platform enables the development of embedded so... Versal ACAPs. It provides a unified programming model for accelerating Edge Design Suite as well. Users can add Vitis Model Composer which is a AMD tool using AMD System Generator for DSP, you can continue development using V...

- Design Tools
  - Vitis Unified Software Platform
    - Vitis
    - Vitis IP Cache (Enable faster on-boarding for new users)
    - Vivado
    - Vitis HLS
    - Vitis Model Composer (Toolbox for MATLAB and Simulink. Includes...)
  - DocNav
- Devices
  - Install devices for Alveo and edge acceleration platforms
  - Install Devices for Kria SOMs and Starter Kits
  - Devices for Custom Platforms
    - SoCs
      - 7 Series
      - UltraScale
      - UltraScale+
      - Versal ACAP
    - Engineering Sample Devices for Custom Platforms
- Installation Options
  - Install Cable Drivers (You MUST disconnect all Xilinx Platform C...

Download Size: NA  
Disk Space Required: 68.45 GB

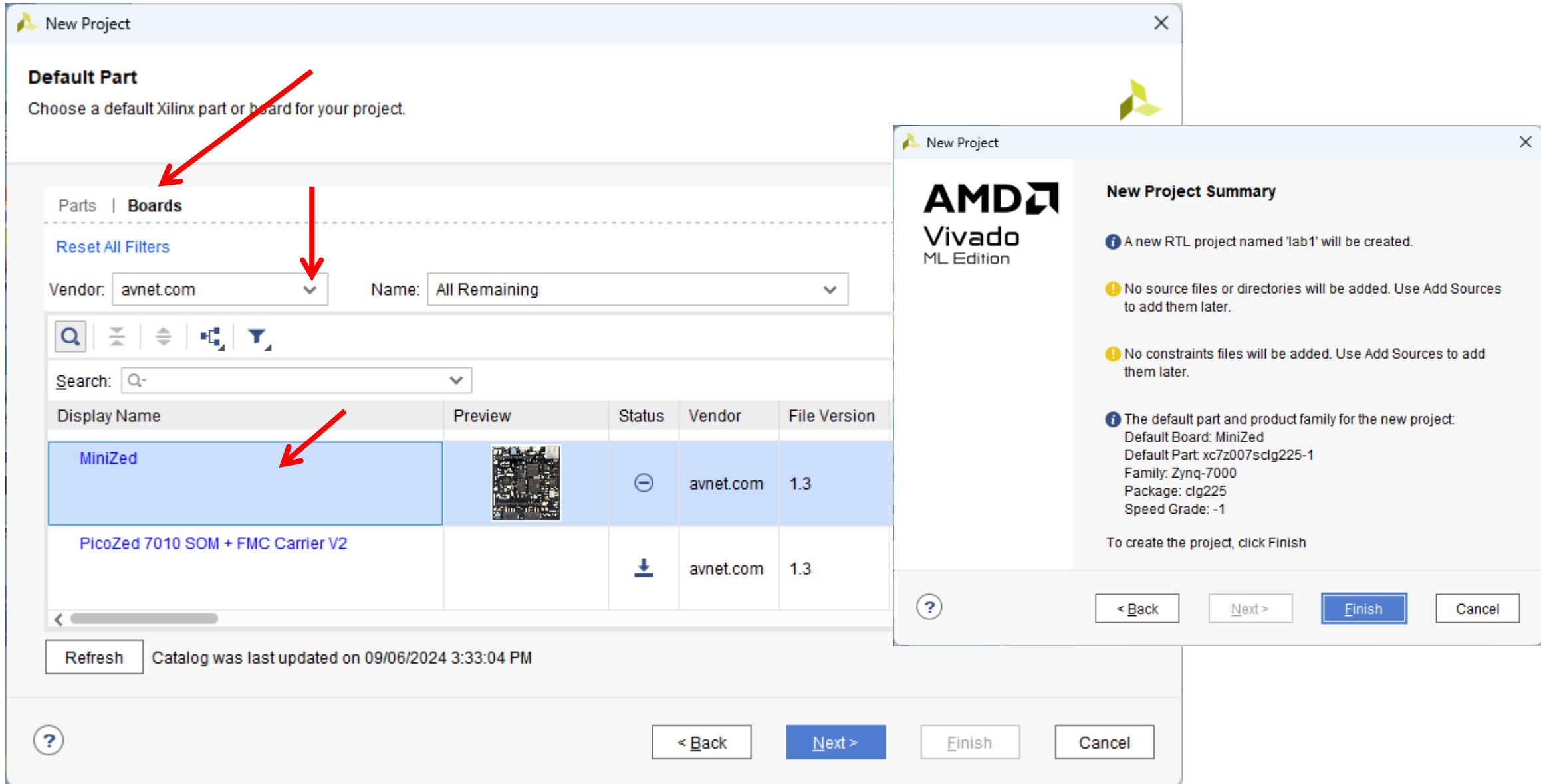


# Vivado 2023 - nov projekt




Vnesemo: ime projektne mape in lokacijo projekta (C:/proj/ime)

Preskočimo dodajanje datotek in zahtev...  
Nastavimo: Default Part (Boards, avnet.com, MiniZed)



The screenshot shows the 'New Project' dialog in Vivado. The 'Default Part' section is active, displaying a list of boards. The 'Boards' tab is selected, and the 'Vendor' is set to 'avnet.com'. The 'Name' dropdown is set to 'All Remaining'. The table below shows the following items:

Display Name	Preview	Status	Vendor	File Version
MiniZed		⊖	avnet.com	1.3
PicoZed 7010 SOM + FMC Carrier V2		↓	avnet.com	1.3

The 'New Project Summary' dialog is overlaid on the right, showing the following details:

**AMD Vivado ML Edition**

**New Project Summary**

- A new RTL project named 'lab1' will be created.
- No source files or directories will be added. Use Add Sources to add them later.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:  
Default Board: MiniZed  
Default Part: xc7z007sclg225-1  
Family: Zynq-7000  
Package: clg225  
Speed Grade: -1

To create the project, click Finish

Buttons: < Back, Next >, Finish, Cancel

# Dodaj opis vezja (Add Sources, design sources)

The image shows the Vivado 2023.1 interface with the 'Add Sources' dialog box open. The 'Add Sources' dialog is titled 'Add Sources' and features the AMD Vivado ML Edition logo. It contains three radio button options: 'Add or create constraints', 'Add or create design sources' (which is selected), and 'Add or create simulation sources'. A red arrow points to the 'Add Sources' option in the Project Manager sidebar. Below the dialog, the 'Add or Create Design Sources' dialog is visible, showing a text input field and three buttons: 'Add Files', 'Add Directories', and 'Create File'. A red arrow points to the 'Create File' button. The 'Add or Create Design Sources' dialog also includes checkboxes for 'Scan and add RTL include files into project', 'Copy sources into project', and 'Add sources from subdirectories' (which is checked). The bottom of the dialog has buttons for '< Back', 'Next >', 'Finish', and 'Cancel'.



# VHDL model

Create Source File

Create a new source file and add it to your project.

File type:  VHDL

File name:

File location:

Define Module

Define a module and specify I/O Ports to add to your source file.  
For each port specified:  
MSB and LSB values will be ignored unless its Bus column is checked.  
Ports with blank names will not be written.

**Module Definition**

Entity name:

Architecture name:

**I/O Port Definitions**

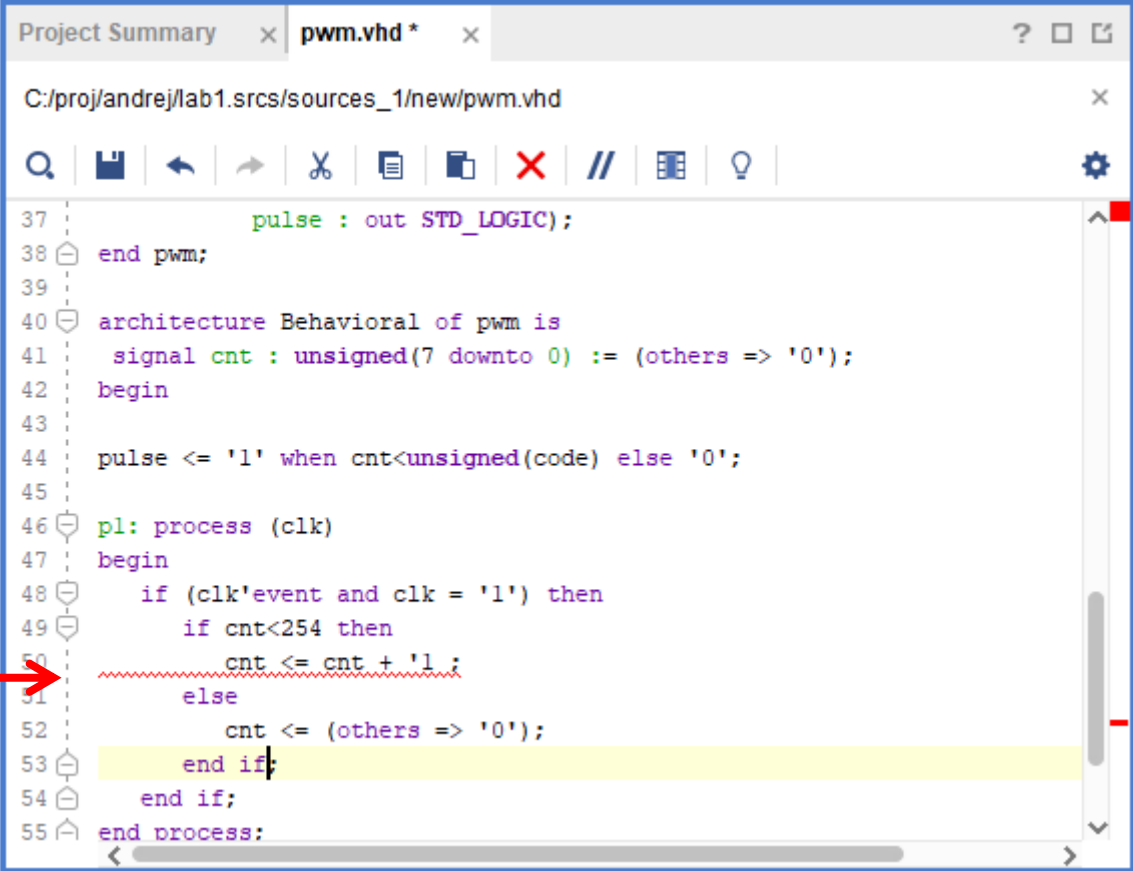
Port Name	Direction	Bus	MSB	LSB
clk	in	<input type="checkbox"/>	0	0
code	in	<input checked="" type="checkbox"/>	7	0
pulse	out	<input type="checkbox"/>	0	0

# Odpri izvorno kodo pwm.vhd

The screenshot displays the Vivado 2023.1 software interface. The top menu bar includes Reports, Window, Layout, View, and Help. The PROJECT MANAGER - lab1 window is open, showing a tree view of sources. A red arrow points to the 'pwm(Behavioral) (pwm.vhd)' file under Design Sources. Below the tree view is the Source File Properties panel for 'pwm.vhd', showing it is enabled and located at 'C:/proj/andrej/lab1.srscs/sources\_1/new'. The main editor window shows the VHDL code for 'pwm.vhd'. The file path 'C:/proj/andrej/lab1.srscs/sources\_1/new/pwm.vhd' is circled in red, with a red arrow pointing to it and the text 'Kje je datoteka?' (Where is the file?). The code in the editor includes library declarations for IEEE and UNISIM, and the behavioral architecture of the 'pwm' entity.

```
22 library IEEE;  
23 use IEEE.STD_LOGIC_1164.ALL;  
24  
25 -- Uncomment the following library declaration if using  
26 -- arithmetic functions with Signed or Unsigned values  
27 --use IEEE.NUMERIC_STD.ALL;  
28  
29 -- Uncomment the following library declaration if instantiating  
30 -- any Xilinx leaf cells in this code.  
31 --library UNISIM;  
32 --use UNISIM.VComponents.all;  
33  
34 entity pwm is  
35     Port ( clk : in STD_LOGIC;  
36           code : in STD_LOGIC_VECTOR (7 downto 0);  
37           pulse : out STD_LOGIC);  
38 end pwm;  
39  
40 architecture Behavioral of pwm is  
41
```

# Preverjanje sintakse med pisanjem kode



```
Project Summary x pwm.vhd * x ? □ ✕
C:/proj/andrej/lab1.srcs/sources_1/new/pwm.vhd x
🔍 📁 ⏪ ⏩ ✂ 📄 📄 ✖ // 📄 💡 ⚙
37 | pulse : out STD_LOGIC);
38 | end pwm;
39 |
40 | architecture Behavioral of pwm is
41 |   signal cnt : unsigned(7 downto 0) := (others => '0');
42 |   begin
43 |
44 |   pulse <= '1' when cnt<unsigned(code) else '0';
45 |
46 |   p1: process (clk)
47 |   begin
48 |     if (clk'event and clk = '1') then
49 |       if cnt<254 then
50 |         cnt <= cnt + '1';
51 |       else
52 |         cnt <= (others => '0');
53 |       end if;
54 |     end if;
55 |   end process;
```

# Analiza kode: Linter

The screenshot shows the IDE interface with the following components:

- PROJECT MANAGER:** Settings, Add Sources, Language Templates, IP Catalog.
- IP INTEGRATOR:** Create Block Design, Open Block Design, Generate Block Design.
- SIMULATION:** Run Simulation.
- RTL ANALYSIS:** Run Linter (highlighted with a red arrow), Open Elaborated Design.
- SYNTHESIS:** Run Synthesis, Open Synthesized Design.
- IMPLEMENTATION:** Run Implementation, Open Implemented Design.

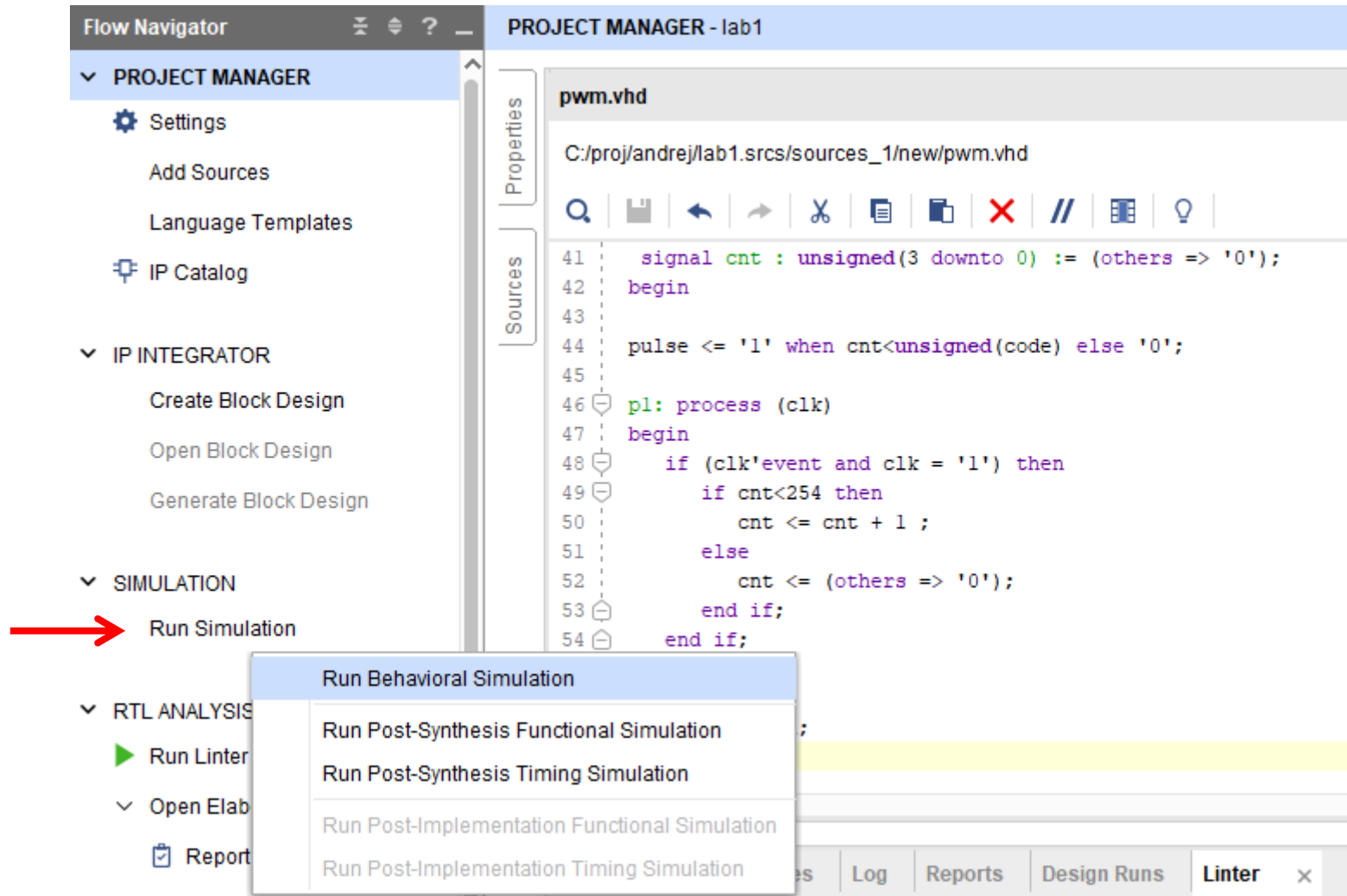
The main editor window displays the code for `pwm.vhd` with the following content:

```
32 --use UNISIM.VComponents.all;
33
34 entity pwm is
35     Port ( clk : in STD_LOGIC;
36           code : in STD_LOGIC_VECTOR (7 downto 0);
37           pulse : out STD_LOGIC);
38 end pwm;
39
40 architecture Behavioral of pwm is
41     signal cnt : unsigned(3 downto 0) := (others => '0');
42 begin
43
44     --pulse <= '1' when cnt<unsigned(code) else '0';
45
46     p1: process (clk)
47     begin
48         if (clk'event and clk = '1') then
49             if cnt<254 then
50                 cnt <= cnt + 1 ;
```

The Linter report window shows the following table of violations:

Rule ID	RTL Name	RTL Hierarchy	Message Body	File Name
ASSIGN-9				
ASSIGN-9# 1	pulse	pwm	Found bit(s) not assigned for IO port 'pulse', first unassigned bit '0'	<a href="#">pwm.vhd : 37</a>
ASSIGN-10				
ASSIGN-10# 1	code	pwm	Found bit(s) not read for IO port 'code', first unread bit '0'	<a href="#">pwm.vhd : 36</a>

# Simulacija

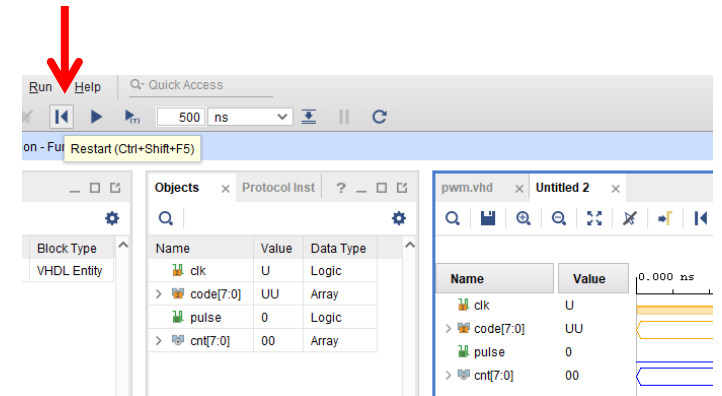


The screenshot shows the 'PROJECT MANAGER - lab1' window. On the left, the 'SIMULATION' folder is expanded, and a red arrow points to 'Run Simulation'. A context menu is open over 'Run Simulation', listing several simulation options. The main editor displays the VHDL code for 'pwm.vhd'.

```
41 signal cnt : unsigned(3 downto 0) := (others => '0');
42 begin
43
44 pulse <= '1' when cnt<unsigned(code) else '0';
45
46 pl: process (clk)
47 begin
48 if (clk'event and clk = '1') then
49 if cnt<254 then
50 cnt <= cnt + 1 ;
51 else
52 cnt <= (others => '0');
53 end if;
54 end if;
```

Simulacija se avtomatsko izvede.

Če ni testne strukture, naredimo Restart



The screenshot shows the simulation window with a red arrow pointing to the 'Restart' button in the top toolbar. The toolbar also includes 'Run' and 'Help' buttons. Below the toolbar, the 'Objects' table is visible.

Name	Value	Data Type
clk	U	Logic
code[7:0]	UU	Array
pulse	0	Logic
cnt[7:0]	00	Array

# Nastavi vhode: ura, Force Clock

SIMULATION - Behavioral Simulation - Functional - sim\_1 - pwm

Scope x Sources

Name	Design Unit	Blc
pwm	pwm(Behavioral)	VH

Objects x Protocol Ins ? \_ □ □

Name	Value	Data Type
clk	U	Logic
> code[7:0]	UU	Array
pulse	U	Logic
> cnt[3:0]	0	Array

pwm.vhd x Untitled 1 x

desni klik

Force Clock: /pwm/clk

Enter parameters below to force the signal to a constant value. Assignments made from within HDL code or any previously applied constant or clock force will be overridden.

Signal name: /pwm/clk

Value radix: Hexadecimal

Leading edge value: 0

Trailing edge value: 1

Starting after time offset: 0ns

Cancel after time offset:

Duty cycle (%): 50

Period: 10ns

OK Cancel

Tcl Console x Messages Log

# Konstanten vhad

SIMULATION - Behavioral Simulation - Functional - sim\_1 - pwm

The screenshot shows the simulation environment with the following components:

- Scope:** Shows the signal `pwm` in the Behavioral VHDL design unit.
- Objects:** A table listing the objects in the design:

Name	Value	Data Type
<code>clk</code>	0	Logic
<code>code[7:0]</code>	05	Array
<code>pulse</code>	U	Logic
<code>cnt[3:0]</code>	0	Array
- Context Menu:** A context menu is open over the `code[7:0]` object, with the `Force Constant...` option selected. A red arrow points to this option with the text "desni klik".
- Force Constant Dialog:** A dialog box titled "Force Constant: /pwm/code" is open. It contains the following fields:
  - Signal name: `/pwm/code`
  - Value radix: Hexadecimal
  - Force value: `5` (highlighted with a red arrow)
  - Starting after time offset: `0ns`
  - Cancel after time offset: (empty)

# Izvedi simulacijo

The screenshot displays a digital logic simulator interface. At the top, a toolbar contains various simulation controls. A red arrow points to the 'Run' button (a play icon), and another red arrow points to the simulation duration input field, which is set to '500 ns'. Below the toolbar, a status bar indicates the simulation is running for 500 ns. The main window shows a timing diagram for a VHDL simulation. The diagram includes a table of signal values and a corresponding waveform.

Name	Value
clk	1
code[7:0]	05
pulse	1
cnt[3:0]	2

The waveform shows a clock signal (clk) as a regular square wave. The 'code[7:0]' signal is a constant high-level signal with the value '05'. The 'pulse' signal is a square wave that is high for a short duration. The 'cnt[3:0]' signal is a counter that increments from 1 to 15 (represented as 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, a, b, c, d, e, f, 0, 1).



# Prikaz vrednosti (zoom, radix)

The screenshot shows a behavioral simulation window titled "SIMULATION - Behavioral Simulation - Functional - sim\_1 - pwm". The main area displays a waveform with a time axis from 0.000 ns to 160.000 ns. A signal named "cnt[3:0]" is highlighted in blue, and its value is shown as "0". A context menu is open over this signal, listing various actions such as Cut, Copy, Paste, Delete, Find, and Waveform Style. The "Radix" option is selected, and a sub-menu is open showing options: Default, Binary, Hexadecimal, Octal, ASCII, and Unsigned Decimal. A red arrow points to the "Unsigned Decimal" option.

Annotations in red:

- "zoom" points to the zoom-in icon in the toolbar.
- "desni klik" points to the right-click on the signal name in the table.
- "zapri simulacijo" points to the close button in the top right corner of the simulation window.
- A red arrow points to the "Unsigned Decimal" option in the radix sub-menu.

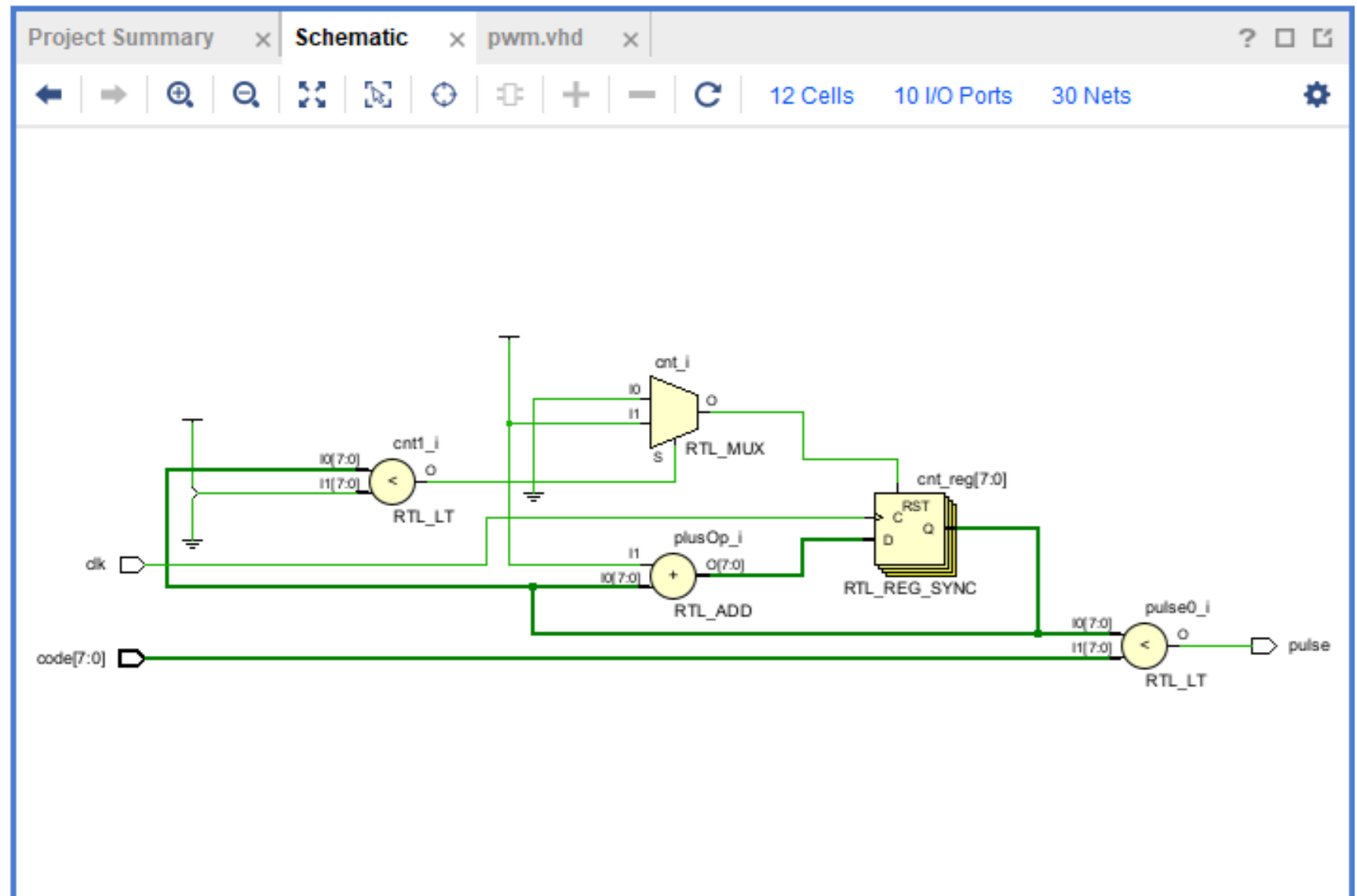
Name	Value
clk	1
code[7:0]	05
pulse	1
cnt[3:0]	0

```
add_force (/pwm/clk) -radix hex {0 0ns} {1 5000ps} -repea
add_force (/pwm/code) -radix hex {5 0ns}
```

# RTL shema (Open Elaborated Design)

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS**
  - Run Linter
  - Open Elaborated Design**
  - Report Methodology
    - Report DRC
    - Report Noise
  - Schematic

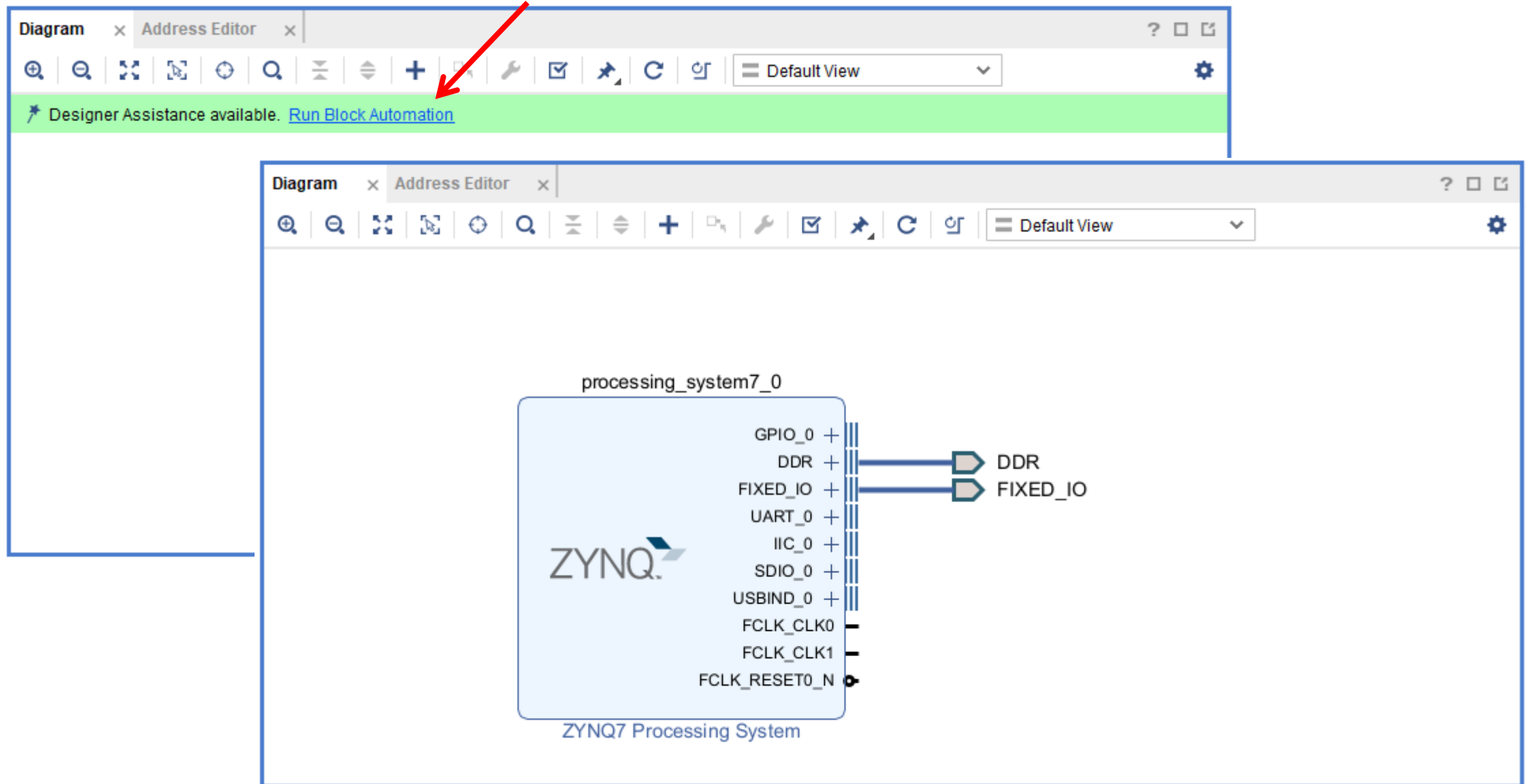




# Blokovni načrt s procesorjem

The screenshot displays the Xilinx Vivado IDE interface for a block design. The top bar indicates the current design is 'BLOCK DESIGN - design\_1\*'. On the left, the 'Flow Navigator' pane is open, showing a tree view with categories: PROJECT MANAGER, IP INTEGRATOR (highlighted), SIMULATION, and RTL ANALYSIS. A red arrow points to the 'Create Block Design' option under the IP INTEGRATOR section. The main workspace is divided into three panes: 'Sources', 'Properties', and 'Diagram'. The 'Sources' pane shows a single source named 'design\_1'. The 'Properties' pane is currently empty, displaying the text 'Select an object to see properties'. The 'Diagram' pane shows a search for 'zyn' with one match: 'ZYNQ7 Processing System'. Below the search results, a message states: 'Design is empty. Press the + button to add IP.'

# Blokovni načrt s procesorjem



# Nastavi Zynq7

The screenshot shows the 'Re-customize IP' dialog for a ZYNQ7 Processing System (5.5). The 'PS-PL Configuration' tab is active, displaying a table of configuration options. A red arrow points to the 'PS-PL Configuration' tab in the left sidebar, and another red arrow points to the 'M AXI GP0 interface' row in the table, which has its checkbox checked.

**ZYNQ7 Processing System (5.5)**

Documentation Presets IP Location Import XPS Settings

**Page Navigator**

- Zynq Block Design
- PS-PL Configuration**
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

**PS-PL Configuration** [Summary Report](#)

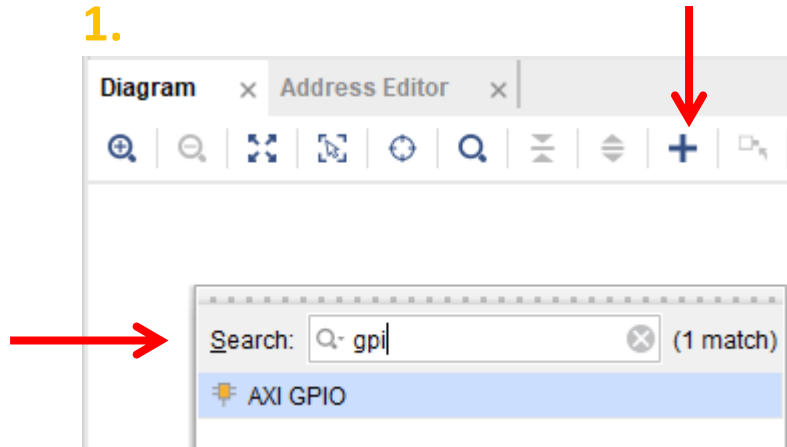
Search: Q-

Name	Select	Description
> General		
> AXI Non Secure Enablement	0	Enable AXI Non Secure Transaction
> GP Master AXI Interface		
> M AXI GP0 interface	<input checked="" type="checkbox"/>	Enables General purpose AXI master interface 0
> M AXI GP1 interface	<input type="checkbox"/>	Enables General purpose AXI master interface 1
> GP Slave AXI Interface		
> HP Slave AXI Interface		
> ACP Slave AXI Interface		
> DMA Controller		
> PS-PL Cross Trigger interface	<input type="checkbox"/>	Enables PL cross trigger signals to PS and vice-versa

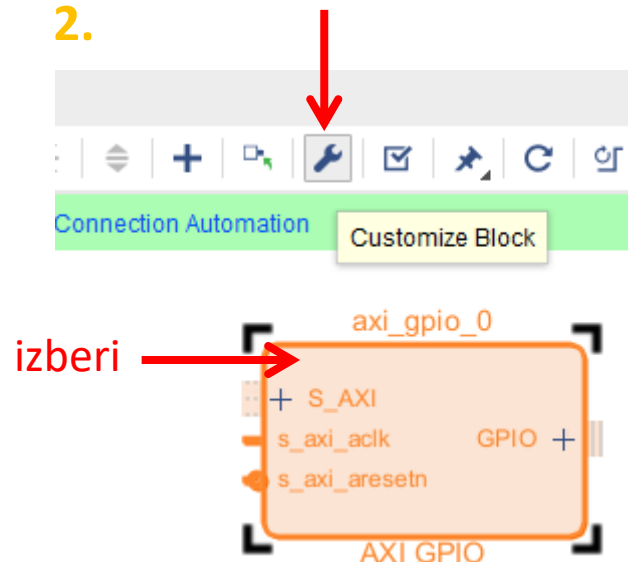
OK Cancel

# Dodaj vmesnik GPIO z 8-bitnim izhodom

1.

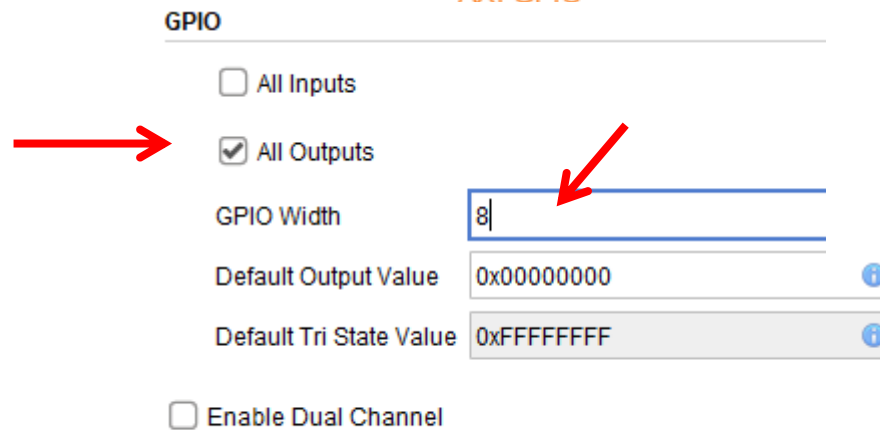


2.

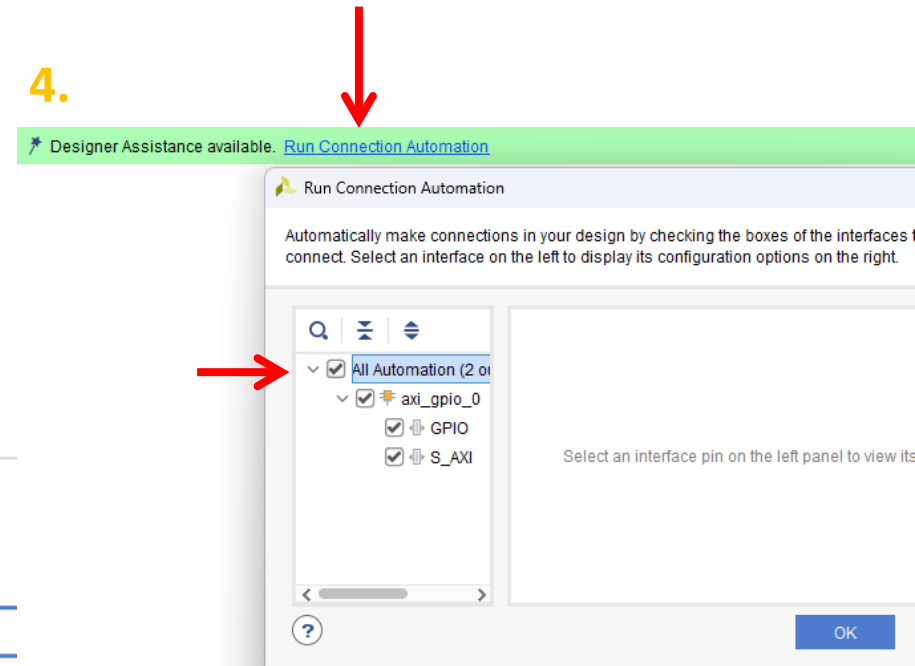


3.

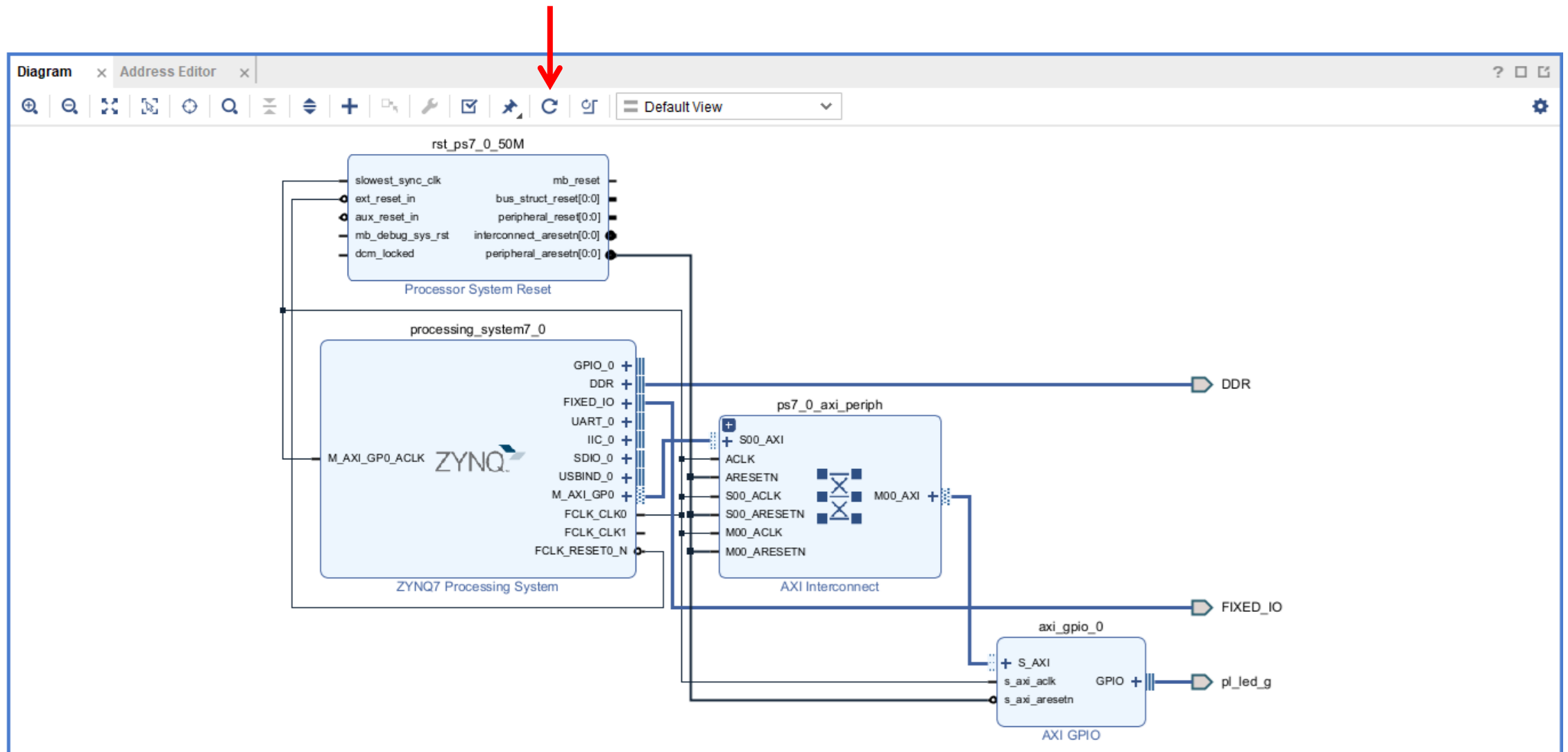
nastavi



4.



# Zynq in GPIO





# Dodajaj VHDL komponento

The screenshot displays the Xilinx Vivado IDE interface for a block design named 'design\_1'. The left sidebar contains the 'PROJECT MANAGER' and 'IP INTEGRATOR' sections. The 'IP INTEGRATOR' section is active, showing options like 'Create Block Design', 'Open Block Design', and 'Generate Block Design'. The main workspace is divided into 'Sources', 'Design', and 'Signals' tabs. The 'Design' tab is active, showing a context menu with options like 'Properties...', 'Delete', 'Copy', 'Paste', 'Search...', 'Select All', 'Add IP...', and 'Add Module...'. The 'Add Module...' option is highlighted with a red arrow. The 'Add Module' dialog box is open, showing a search field and a list of modules. The 'Module type' is set to 'RTL'. The search field contains 'Q-'. The list of modules includes 'pwm (pwm.vhd)', which is selected and highlighted with a red arrow. The dialog box also has 'OK' and 'Cancel' buttons.

Flow Navigator

BLOCK DESIGN - design\_1

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Run Linter
- Open Elaborated Design

Sources

Design x

Signals

design\_1

Diagram

Default View

Properties

Select an object to see properties

Tcl Console

Messages

Log

Reports

Design Runs

Add Module

Select a module to add to the block design.

Module type: RTL

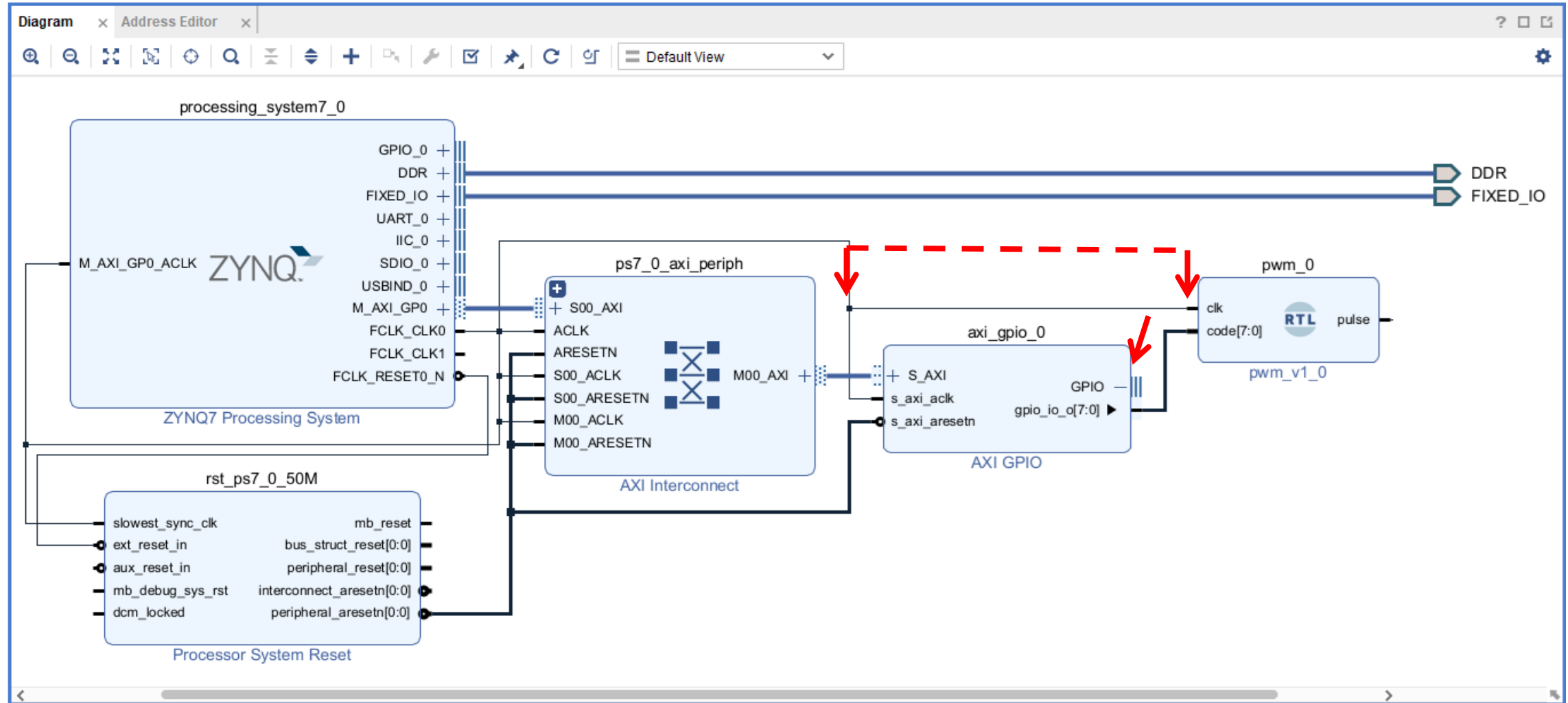
Search: Q-

pwm (pwm.vhd)

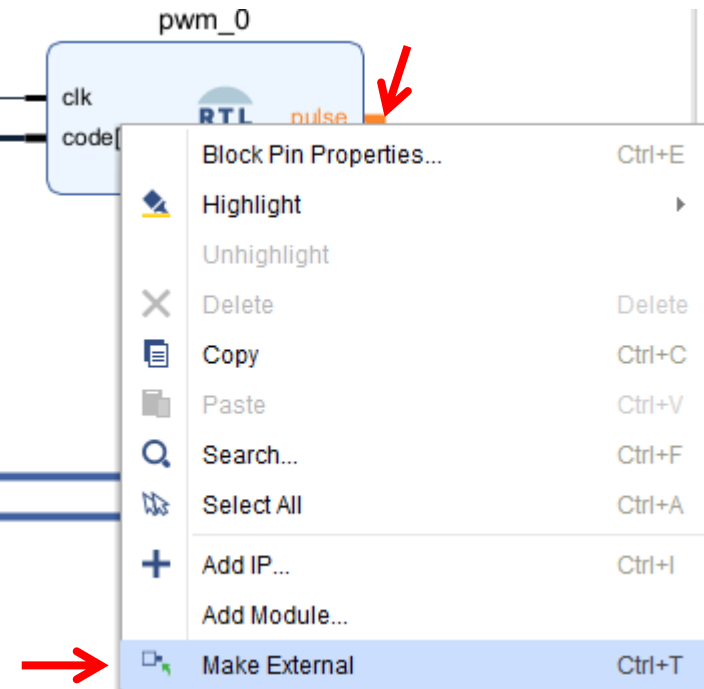
OK

Cancel

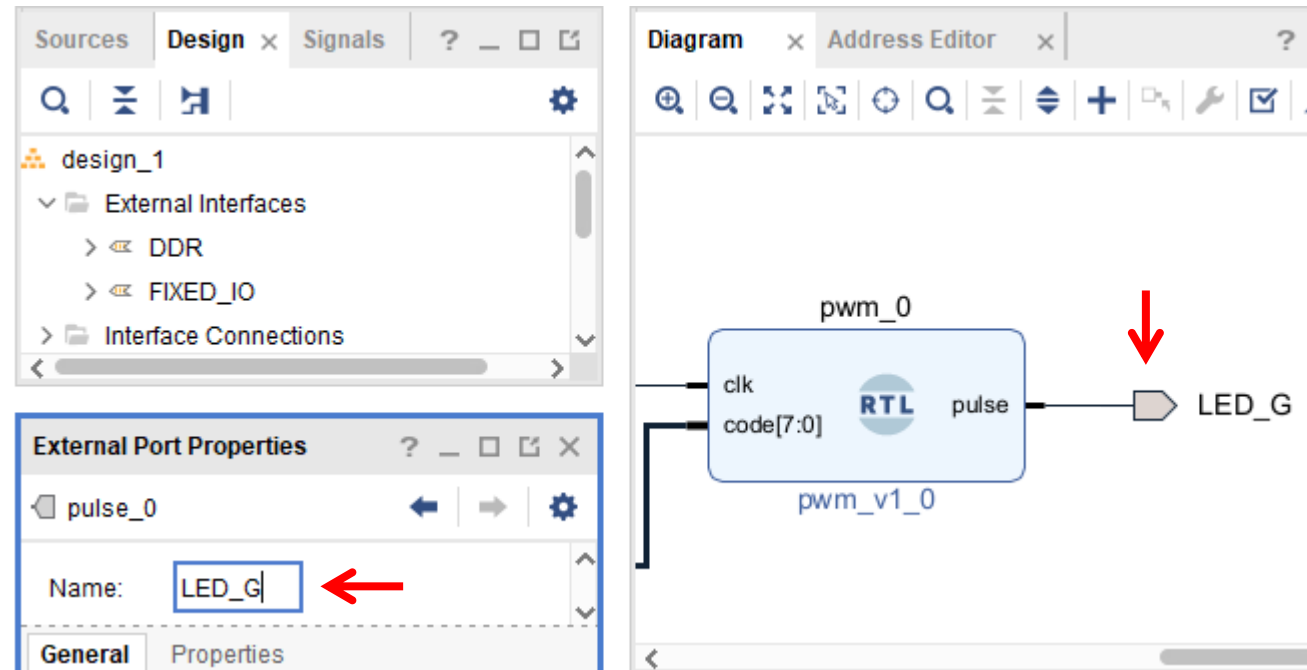
# Ročno poveži



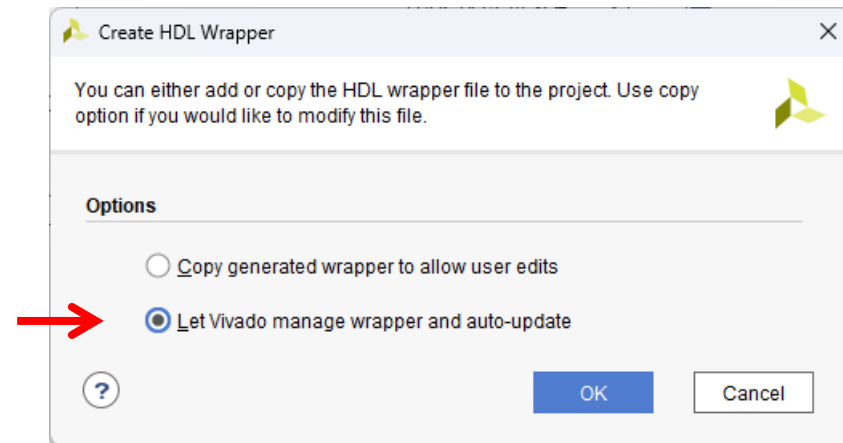
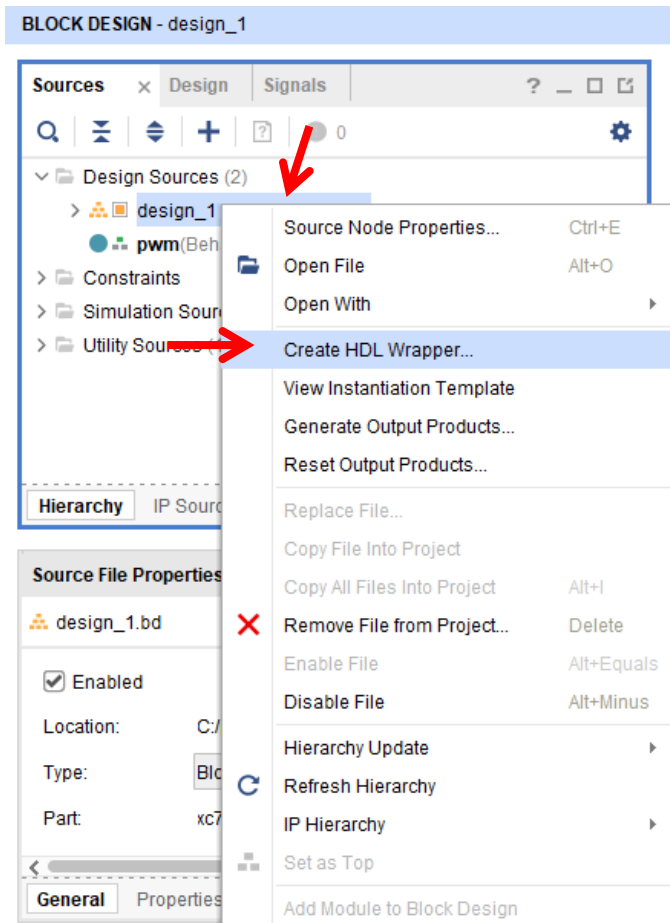
# Dodaj priključek



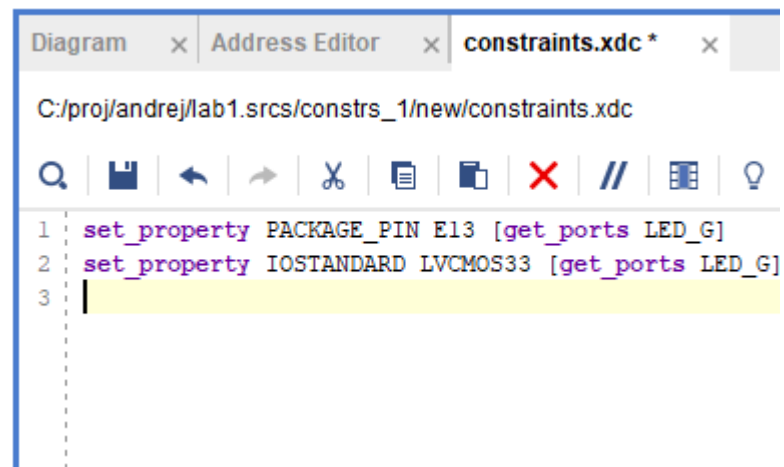
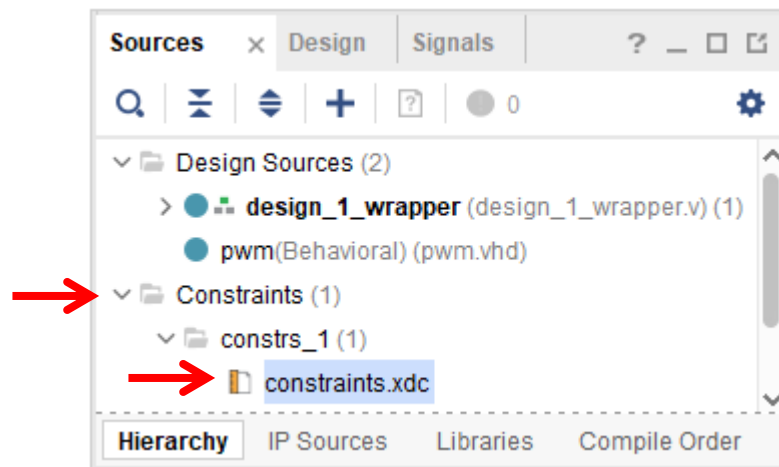
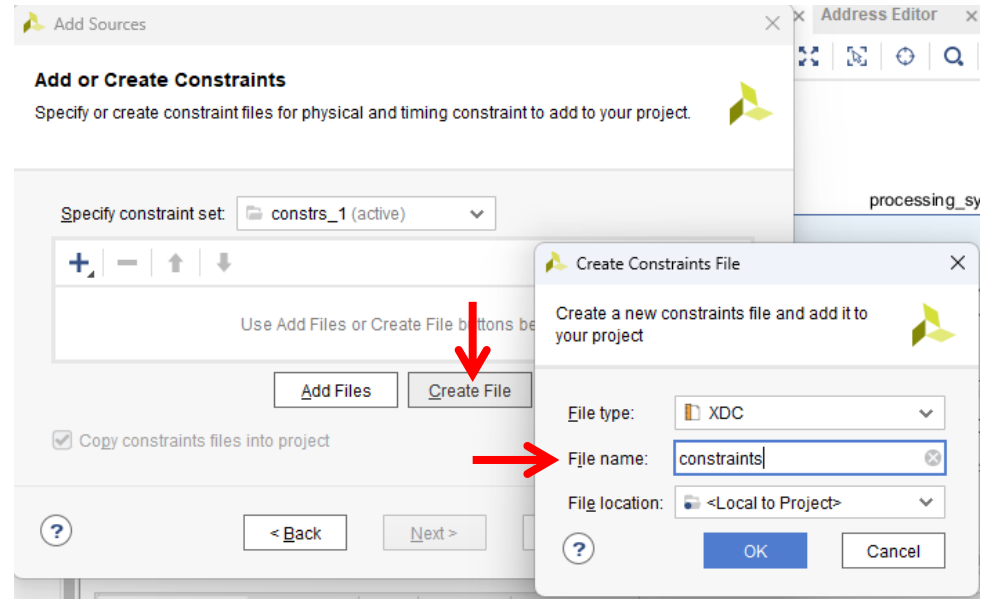
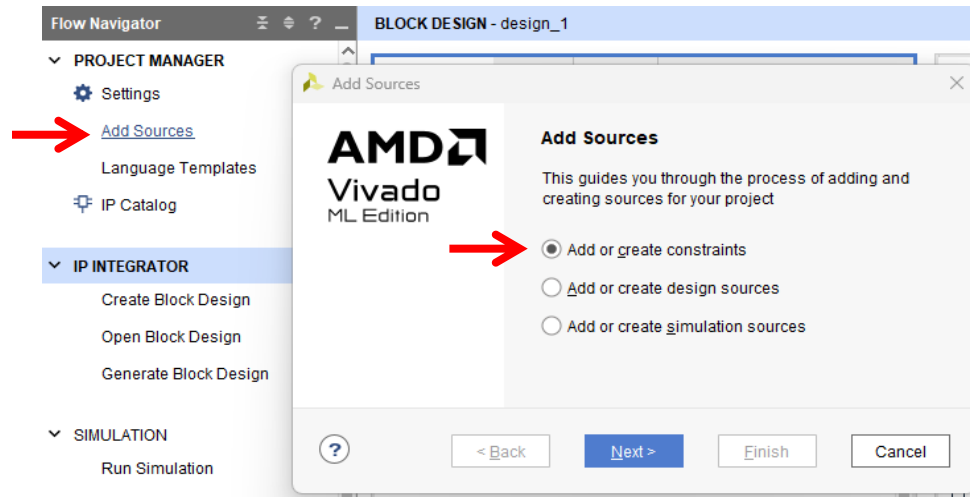
priključek pulse\_0 preimenuj v LED\_G



# Pretvori blokovni načrt v HDL



# Nastavitve priključkov



# Prevajanje: sinteza, implementacija

**Run Implementation** (highlighted in the left sidebar)

**Sources**

- Design Sources (2)
  - design\_1\_wrapper** (design\_1\_wrap) (highlighted as the main source file)
  - pwm(Behavioral) (pwm.vhd)
- Constraints (1)
  - constrs\_1 (1)
    - constraints.xdc

**Source File Properties**

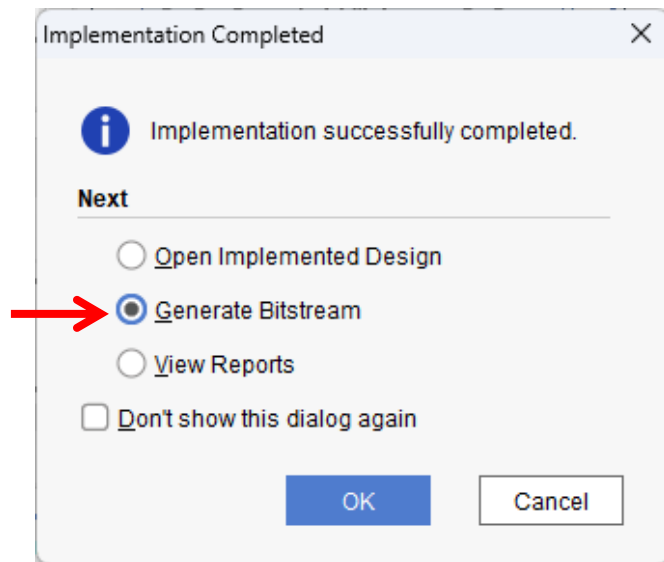
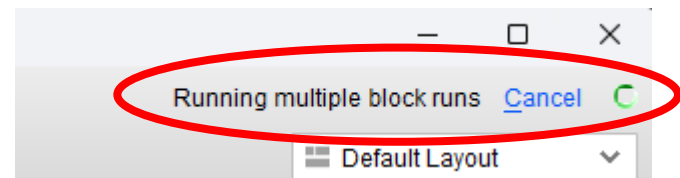
design\_1\_wrapper.v

Enabled

Location: c:/proj/andrej/lab1.gen/source

**Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS
synth_1 (active)	constrs_1	synth_design Complete!					
impl_1	constrs_1	Running opt_design...					
Out-of-Context Module Runs							
design_1		Submodule Runs Complete					
design_1_processing_system7_0_0_synth_1	design_1_pro	synth_design Complete!					
design_1_axi_gpio_0_0_synth_1	design_1_axi	synth_design Complete!					
design_1_auto_pc_0_synth_1	design_1_au	synth_design Complete!					
design_1_rst_ps7_0_50M_0_synth_1	design_1_rst	synth_design Complete!					
design_1_pwm_0_2_synth_1	design_1_pw	synth_design Complete!					



# Rezultat

Project Summary x Device x constraints.xdc x

Overview | Dashboard

### Synthesis

Status: ✔ Complete  
Messages: ! 1 critical warning  
! 354 warnings  
Active run: synth\_1  
Part: xc7z007sclg225-1  
Strategy: Vivado Synthesis Defaults  
Report Strategy: Vivado Synthesis Default Reports  
Incremental synthesis: Automatically selected checkpoint

### DRC Violations

No DRC violations were found.  
[Implemented DRC Report](#)

### Utilization

Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization
LUT	3%
LUTRAM	1%
FF	2%
IO	2%
BUFG	3%

Sources Netli x ? \_ □ □

- design\_1\_wrapper
  - Nets (88)
  - Leaf Cells (1)
  - design\_1\_i (design\_1)

Source File ? \_ □ □ X

Select an object to see properties

Project Summary x Device x constraints.xdc x

Tcl Console Messages Log Reports Design Runs Methodology Power Timing x ? \_ □ □

### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 12,832 ns	Worst Hold Slack (WHS): 0,055 ns	Worst Pulse Width S
Total Negative Slack (TNS): 0,000 ns	Total Hold Slack (THS): 0,000 ns	Total Pulse Width N
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing E
Total Number of Endpoints: 1271	Total Number of Endpoints: 1271	Total Number of End

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved)