

DIVS –Vivado debugiranje

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Laboratorij za načrtovanje integriranih vezij



Virtual Input/Output

- JTAG vmesnik za opazovanje in nastavljanje signalov v vezju FPGA med delovanjem
- nadomešča digitalna stikala in LED (počasni signali)

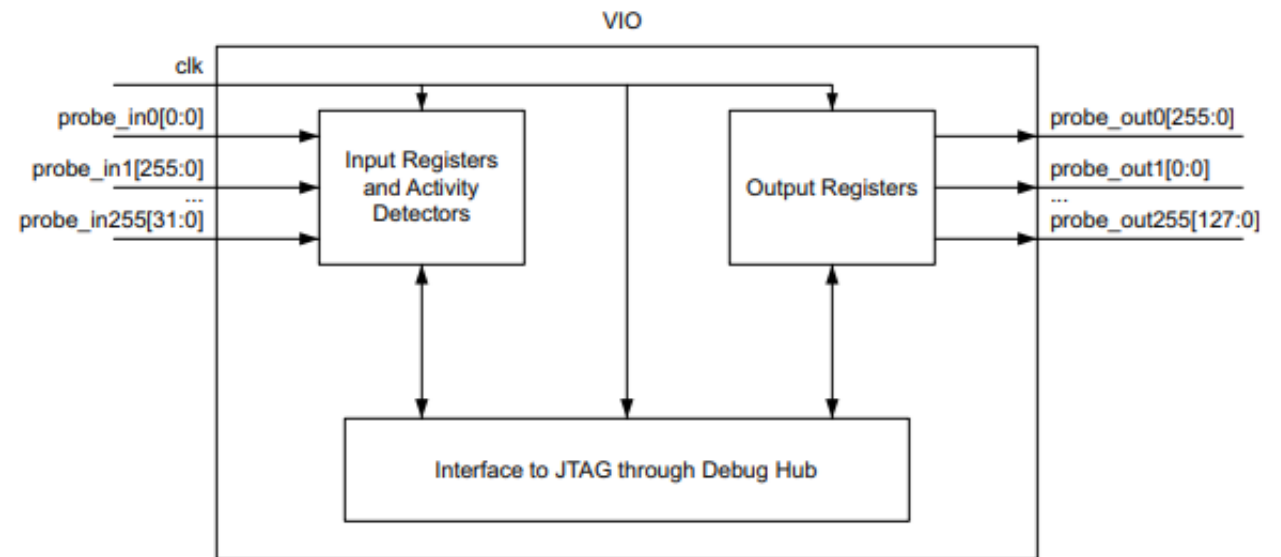
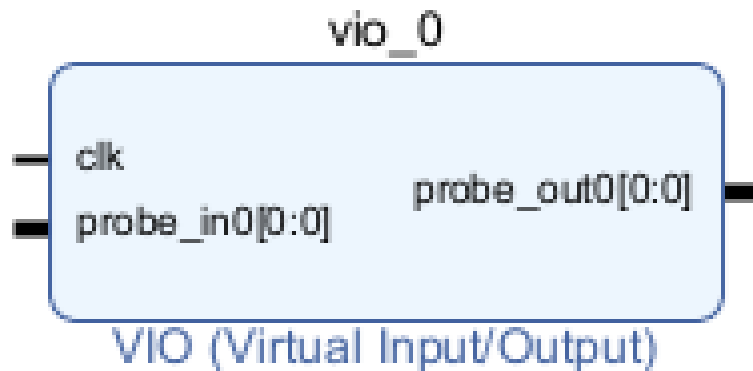
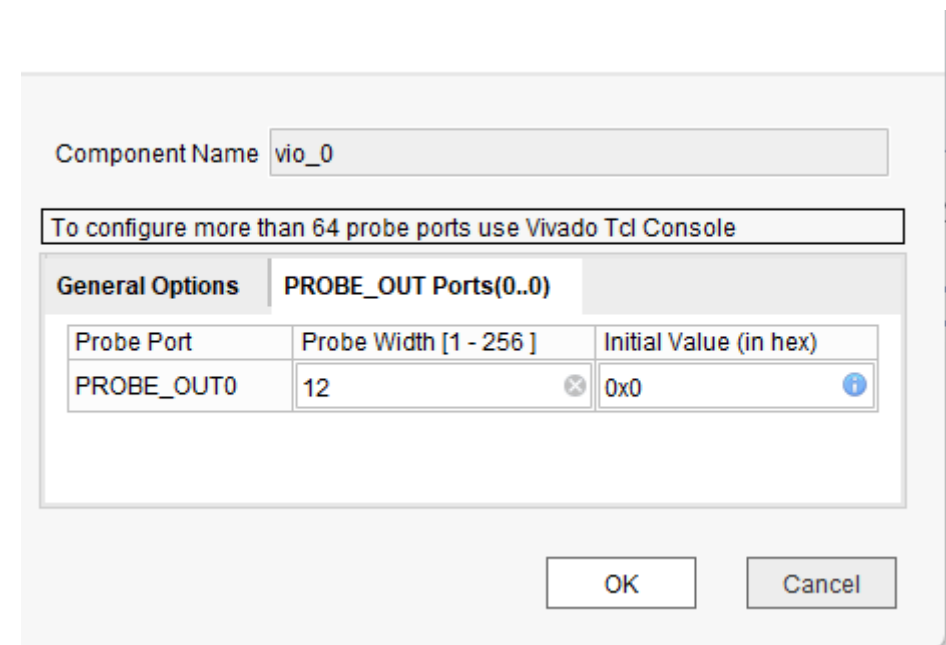
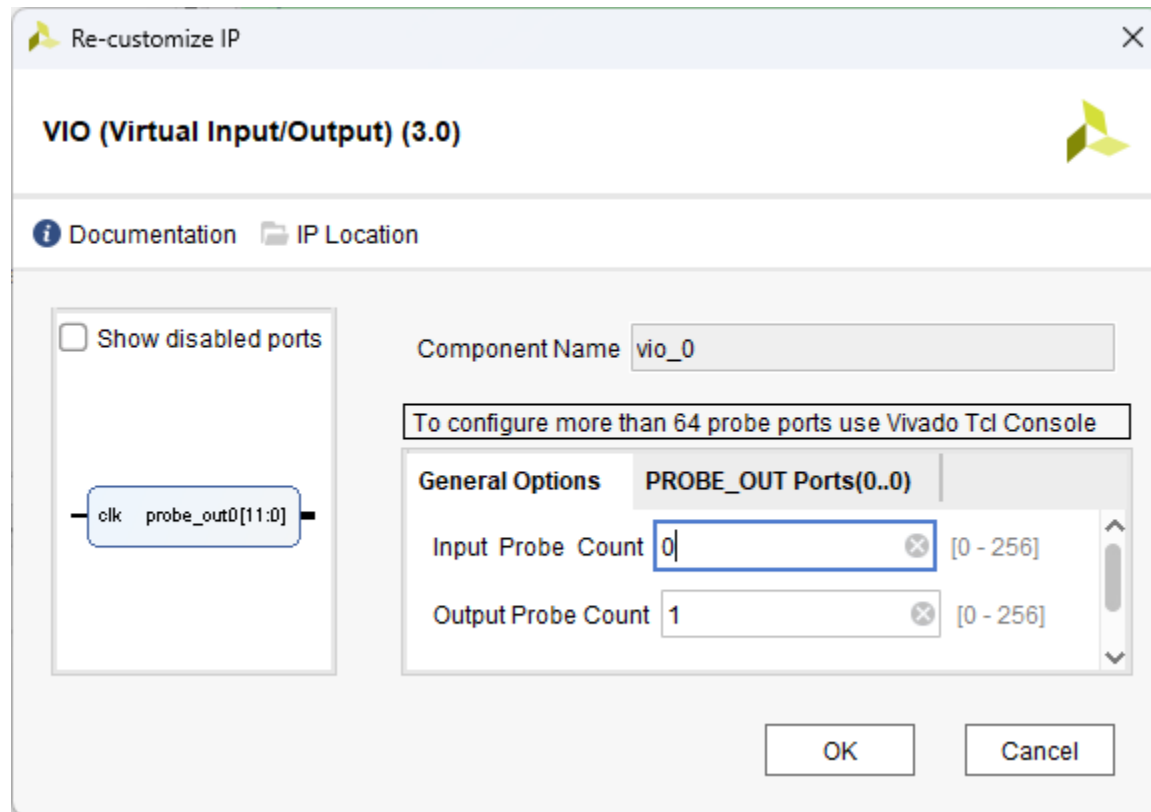


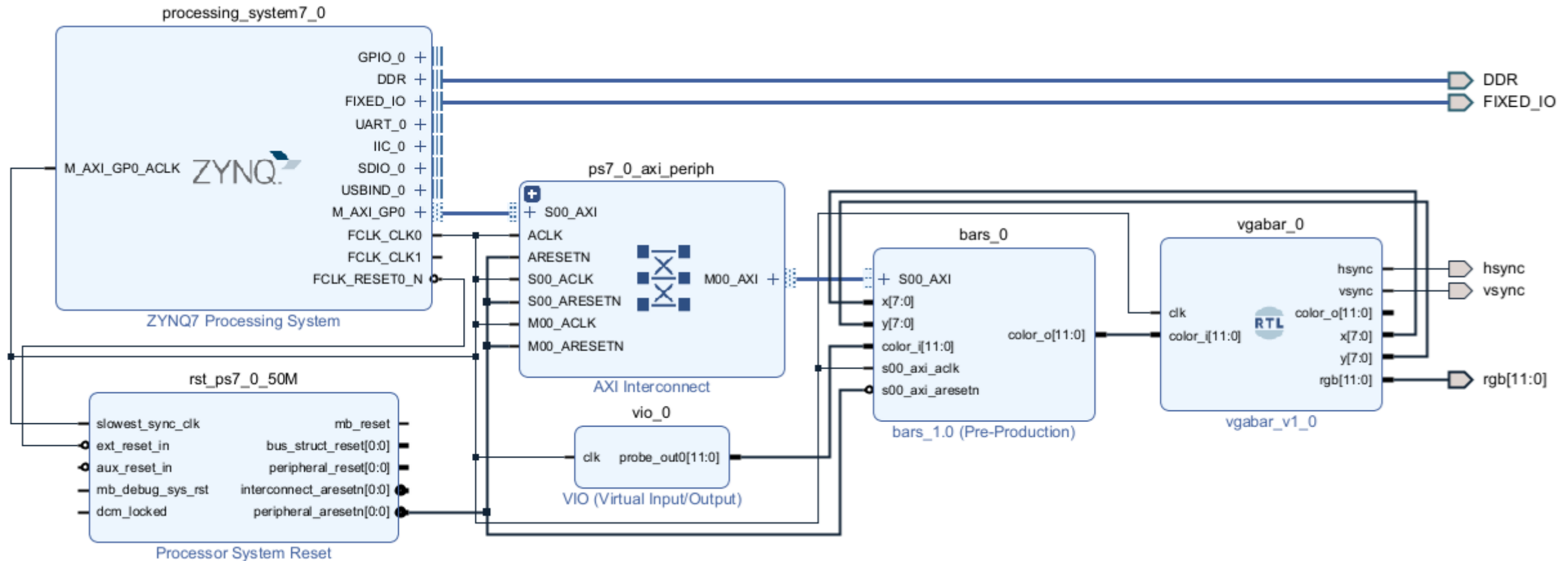
Figure 1-1: VIO Block Diagram

VIO parametri

- Določimo število navideznih vhodov in izhodov in za širino vsakega



Npr: VIO za nastavljjanje barve ozadja



Vivado Hardware Manager

The screenshot shows the Vivado Hardware Manager interface. The top bar displays "HARDWARE MANAGER - unconnected". A green notification bar states "No hardware target is open. Open target". The main area is titled "Hardware" and contains "No content". Below this is a "Properties" panel with the text "Select an object to see properties". At the bottom, the "Tcl Console" shows the following log messages:

```
INFO: [Project 1-1918] Creating Hardware Platform: C
INFO: [Project 1-1943] The Hardware Platform can be
INFO: [Project 1-1941] Successfully created Hardware
INFO: [Hsi 55-2053] elapsed time for repository (C:/
```

On the left, the "PROGRAM AND DEBUG" menu is highlighted, with "Open Hardware Manager" selected. A context menu is open over the "Hardware" panel, showing options: "Auto Connect", "Recent Targets", "Available Targets on Server", and "Open New Target...".

The screenshot shows the Vivado Hardware Manager interface with a connected hardware target. The top bar displays "HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/1234-oj1A". The main area is titled "Hardware" and contains a table with the following data:

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/1234-oj1A (2)	Open
arm_dap_0 (0)	N/A
xc7z007s_1 (3)	Programmed
XADC (System Monitor)	
hw_vio_1 (design_1_iVio_0)	OK - Outputs F

Nastavitev izhodne vrednosti VIO

The screenshot shows the Vivado 2023.1 interface. The Hardware Manager window is active, displaying the hardware configuration for 'localhost/xilinx_tcf/Xilinx/1234-oj1A'. The hardware list includes 'xc7z007s_1 (3)', 'XADC (System Monitor)', 'hw_ila_1 (design_1_i/system_ila_0/U0/probe3_1)', and 'hw_vio_1 (design_1_i/vio_0)'. The 'hw_vio_1' component is selected, and its 'Dashboard Options' are visible. A table lists the VIO configuration:

Name	Value	Acti...	Directi...	VIO
> design_1_i/vio_0_probe_out0[11:0]	[H] 123		Output	hw_vio_1

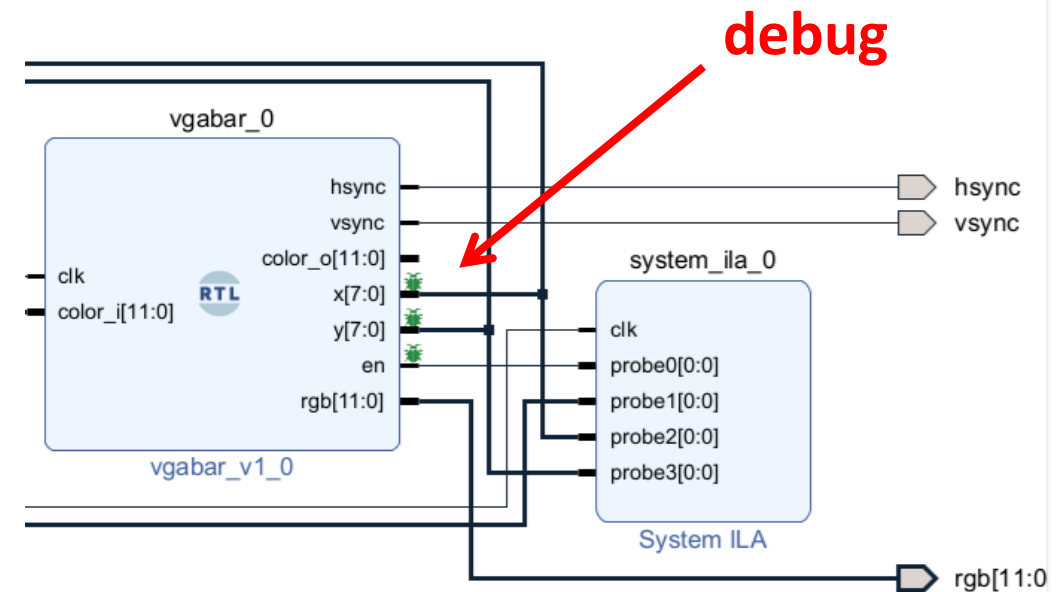
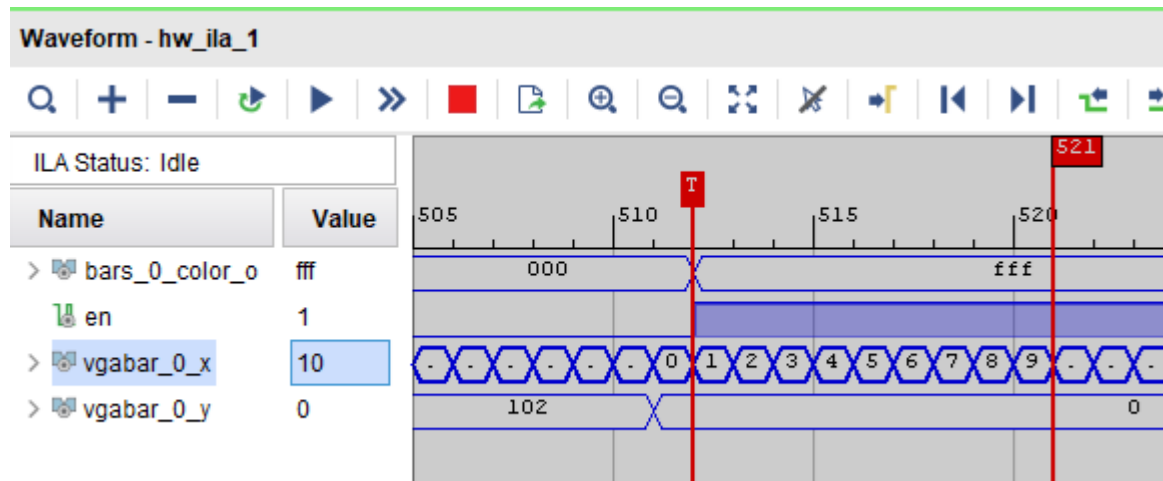
A dialog box is open to edit the 'Value' for the selected VIO. The value is currently '123'. The dialog has 'OK' and 'Cancel' buttons. Red arrows point to the '+' icon in the dashboard options and the 'Value' field in the dialog.

The Tcl Console at the bottom shows the following commands and output:

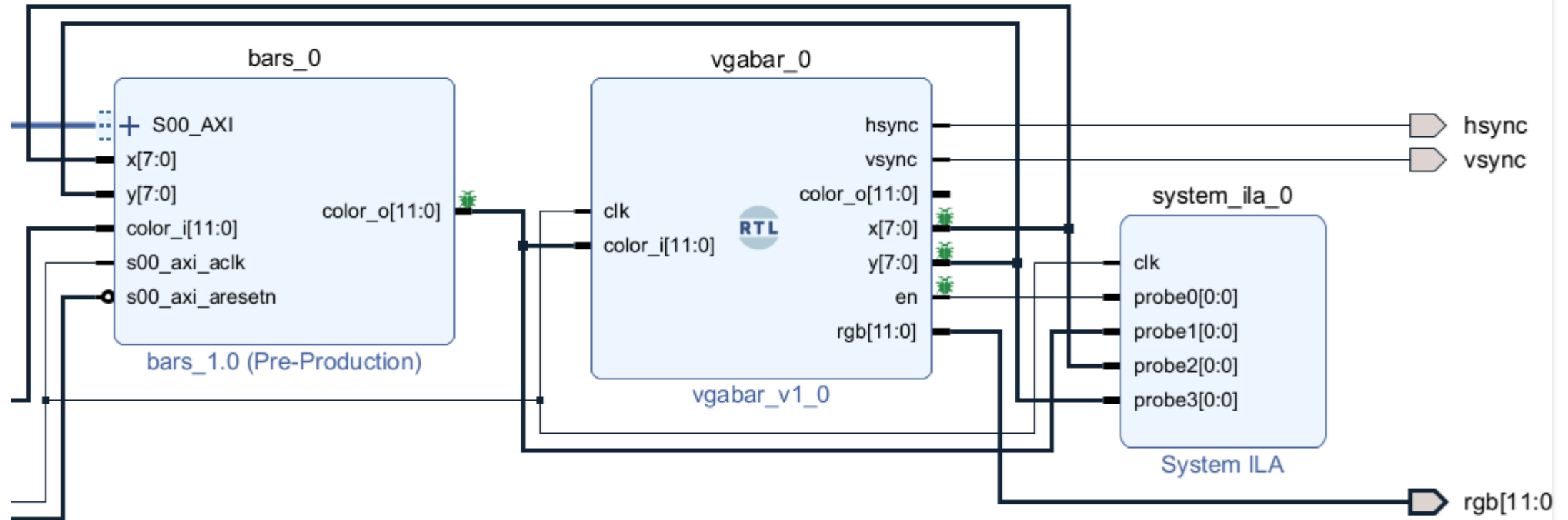
```
INFO: [Labtools 27-1966] The ILA core 'hw_ila_1' triggered at 2024-Nov-04 10:36:21
INFO: [Labtools 27-3304] ILA Waveform data saved to file C:/proj/andrej/divs3/divs3.hw/backup/hw_ila_data_1.ila. Use Tcl command 'read_f
add_wave -into {hw_ila_data_1.wcfg} -radix hex { {design_1_i/system_ila_0/U0/probe3_1} }
set_property NAME.CUSTOM vgabar_0_y [get_hw_probes design_1_i/system_ila_0/U0/probe3_1]
set_property OUTPUT_VALUE 123 [get_hw_probes design_1_i/vio_0_probe_out0 -of_objects [get_hw_devices xc7z007s_1] -filter {CEI
commit_hw_vio [get_hw_probes {design_1_i/vio_0_probe_out0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z007s_1] -filter {CEI
```

Vivado ILA – integrirani logični analizator

- Zajem hitrih signalov ob prožilnem pogoju, prenos podatkov po JTAG in prikaz v obliki časovnega diagrama (waveform)
- npr. zajem in prikaz 1k vzorcev z uro clk



Debagiranje vgabar



- v vgabar.vhd dodamo izhod en, ki je 1, ko smo znotraj okna s stolpci
- nastavimo debug na opazovane signale in prevedemo vezje

Dodajanje signalov in proženja

The image shows a multi-panel screenshot of the Xilinx Hardware Manager interface. The top-left panel displays the hardware tree with 'hw_ila_1' selected. The top-right panel shows the waveform viewer for 'hw_ila_1' with an 'Add Probes' dialog box listing signals like 'bars_0_color_o', 'en', 'vgabar_0_x', and 'vgabar_0_y'. The bottom-left panel shows the 'Status' window with 'Core status' at 'Idle'. The bottom-right panel shows the 'Trigger Setup' window for 'hw_ila_1' with a table of trigger conditions.

Name	Operator	Radix	Value	Port
en	==	[B]	R (0-to-1 transition)	probe0[0]

Additional details from the Trigger Setup window:
0 (logical zero)
1 (logical one)
X (don't care)
R (0-to-1 transition)

Pregled zajetih signalov

The screenshot shows the Xilinx ILS interface for the hw_ila_1 component. The main window displays a waveform capture with a red trigger line at time 512. The signal values are shown in hexadecimal and binary. Below the waveform, there are panels for 'Settings - hw_ila_1' and 'Trigger Setup - hw_ila_1'.

Waveform - hw_ila_1

ILA Status: Idle

Name	Value
bars_0_color_o	123
en	1
vgabar_0_x	23
vgabar_0_y	1

Time: 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534

Signal values: fff, 123, fff, 123

Binary values: 15, 16, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23

Binary values: 2, 1

Settings - hw_ila_1

Core status: Idle

Capture status - Window 1 of 1

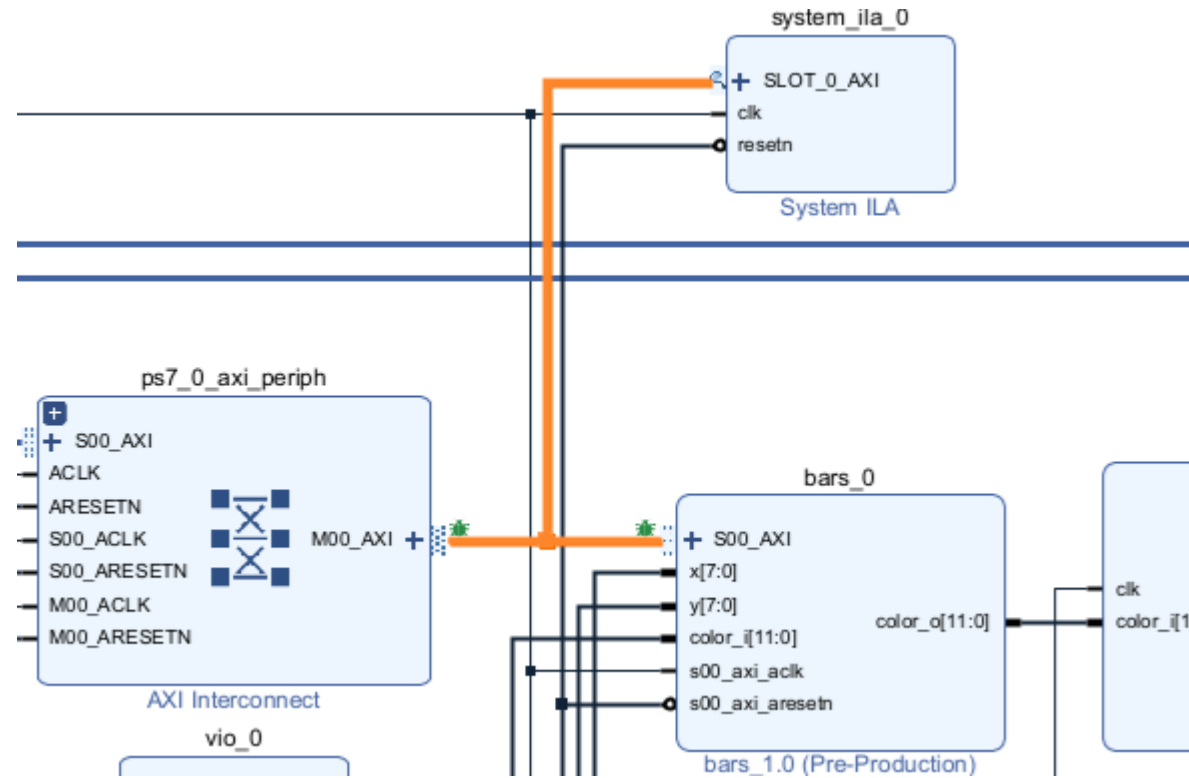
Window sample 0 of 1024

Idle

Trigger Setup - hw_ila_1

Name	Operator	Radix	Value	Port	Comparator Usage
en	==	[B]	R	probe0[0]	1 of 1
vgabar_0_y	==	[H]	01	probe3[7:0]	1 of 1

Opazovanje vodila AXI z ILA



Zajem transakcij na vodilu AXI

HARDWARE MANAGER - localhost/xilinx_tcf/Xilinx/1234-oj1A

Hardware

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/1234-oj1A (2)	Open
arm_dap_0 (0)	N/A
xc7z007s_1 (3)	Programmed
XADC (System Monitor)	
hw_ila_1 (design_1_i/system_ila_0/U0/ila_0)	Idle
hw_vio_1 (design_1_i/vio_0)	OK - Outputs F

ILA Core Properties

hw_ila_1

Name: hw_ila_1
Cell: design_1_i/system_ila_0/U0/ila_0
Device: xc7z007s_1
HW core: core_1

Waveform - hw_ila_1

ILA Status: Idle

Name	Value
slot_0 : ps7_0_axi_periph_M00_AXI : R Channel	No Read
slot_0 : ps7_0_axi_periph_M00_AXI : AW Channel	-
slot_0 : ps7_0_axi_periph_M00_AXI : W Channel	-
slot_0 : ps7_0_axi_periph_M00_AXI : WVALID	0
slot_0 : ps7_0_axi_periph_M00_AXI : WREADY	0
slot_0 : ps7_0_axi_periph_M00_AXI : WDATA	000076a0
slot_0 : ps7_0_axi_periph_M00_AXI : WSTRB	1

Trigger Setup - hw_ila_1

Name	Operator	Radix	Value	Port	Co
design_1_i/system_ila_0/U0/net_slot_0_axi_w_ctrl[1:0]	==	[B]	11	probe14[1:0]	1 c

Vitis – poganjanje SW brez reprogramiranja FPGA

The screenshot displays the Vitis IDE interface with the 'Run Configurations' dialog box open. The dialog is titled 'Create, manage, and run configurations' and is currently showing the 'Target Setup' tab. The configuration name is 'Debugger_test-Default'. The 'Hardware Platform' is set to '\$(sdxTcfLaunchFile:proj)'. The 'Bitstream File' is set to '_ide/bitstream/design_1'. The 'PL Device' and 'PS Device' are both set to 'Auto Detect'. The 'Initialization File' is set to '_ide/psinit/ps7_init.tcl'. The 'Summary' section lists the following operations: 1. Sources the init tcl file (C:\proj\divs3\sw\test_ide\psinit\ps7_init.tcl). 2. Runs ps7_init to initialize PS. 3. Runs ps7_post_config. Enables level shifters from PL to PS. (Recommended to use this option only after system reset or board power ON). The 'Reset entire system' and 'Program FPGA' checkboxes are unchecked, while 'Run ps7_init' and 'Run ps7_post_config' are checked. Red arrows point to the 'Run Configurations...' menu item in the IDE, the 'Debugger_test-Default' entry in the list, and the 'Reset entire system' and 'Program FPGA' checkboxes.