DIVS –Vivado debagiranje

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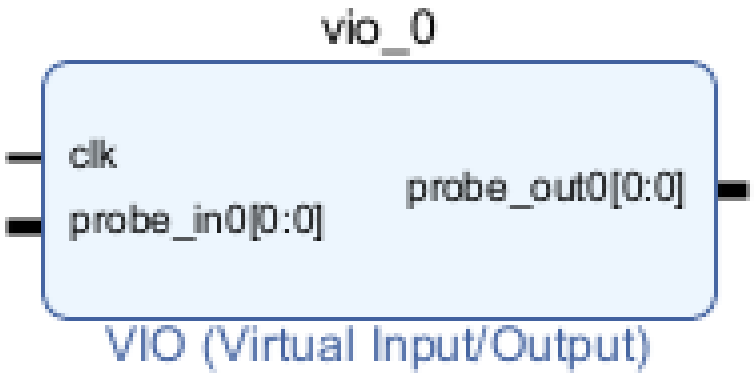
Virtual Input/Output

- JTAG vmesnik za opazovanje in nastavljanje signalov v vezju FPGA med delovanjem
- nadomešča digitalna stikala in LED (počasni signali)



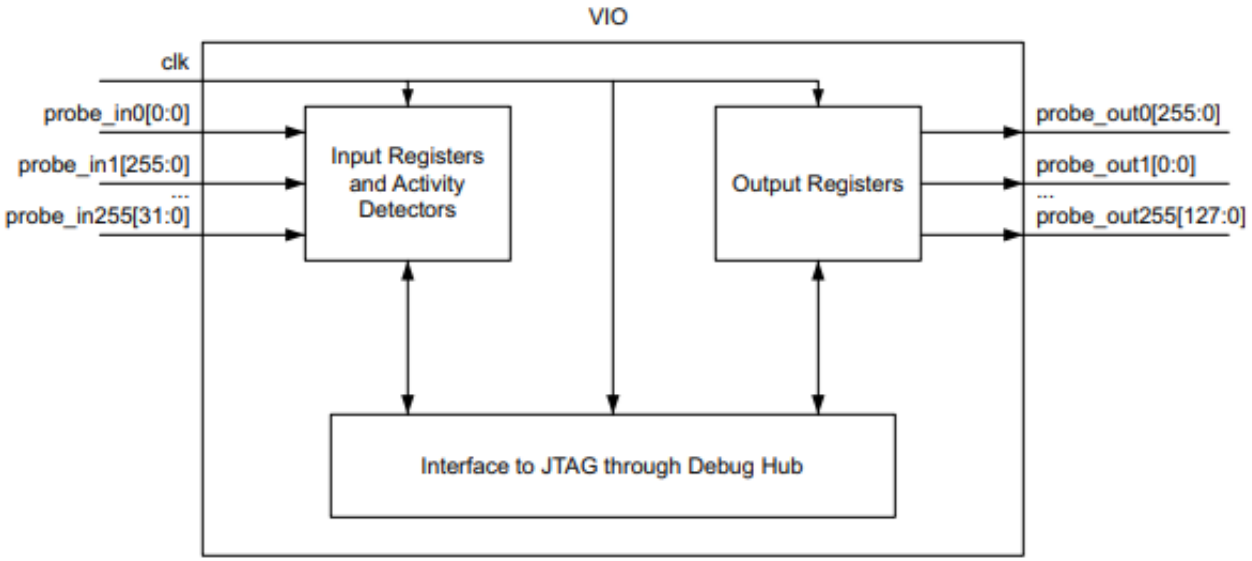
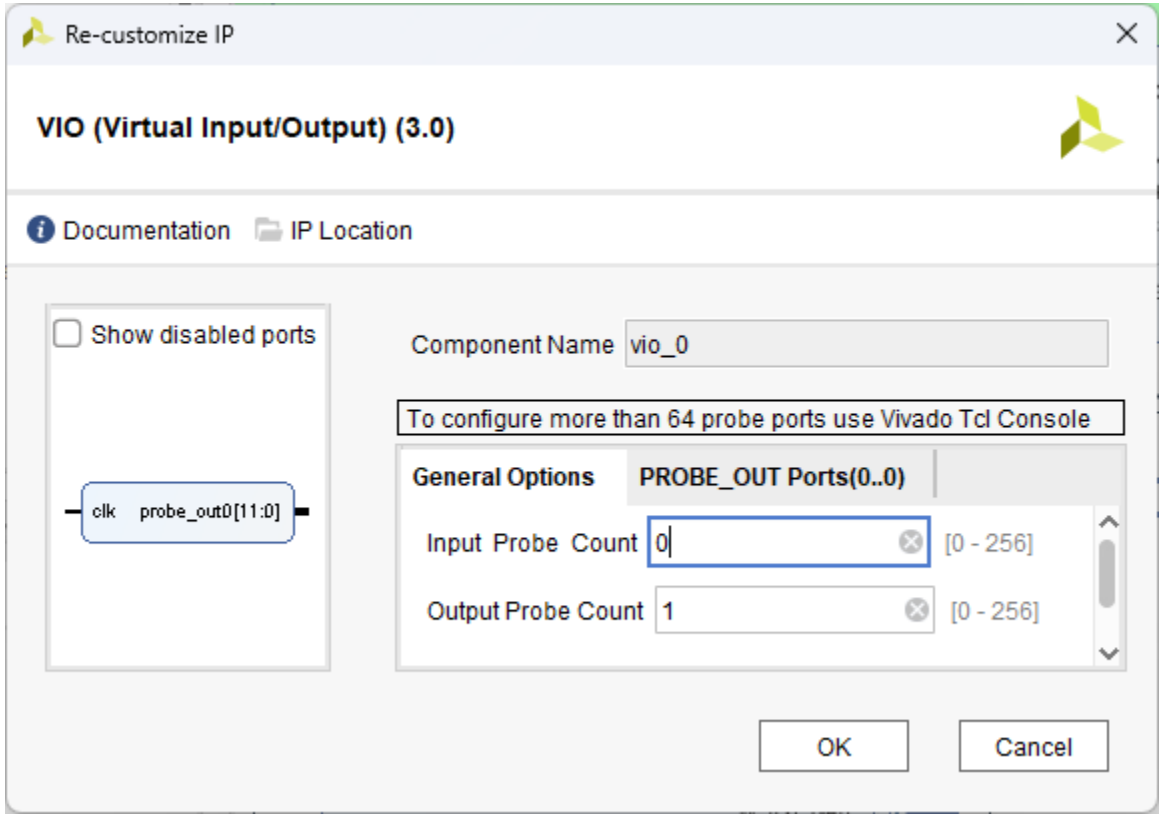
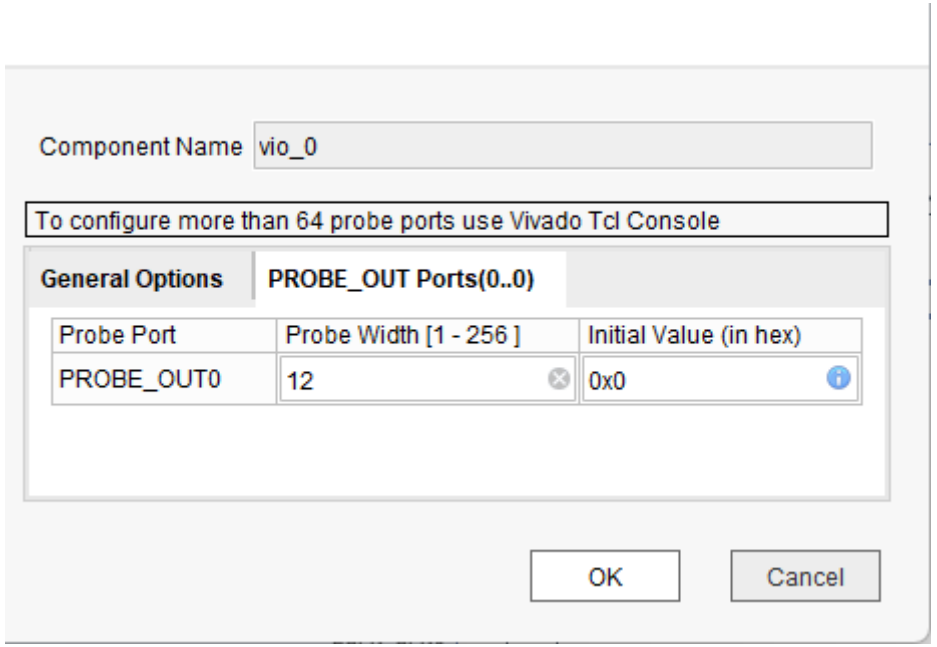


Figure 1-1: **VIO Block Diagram**

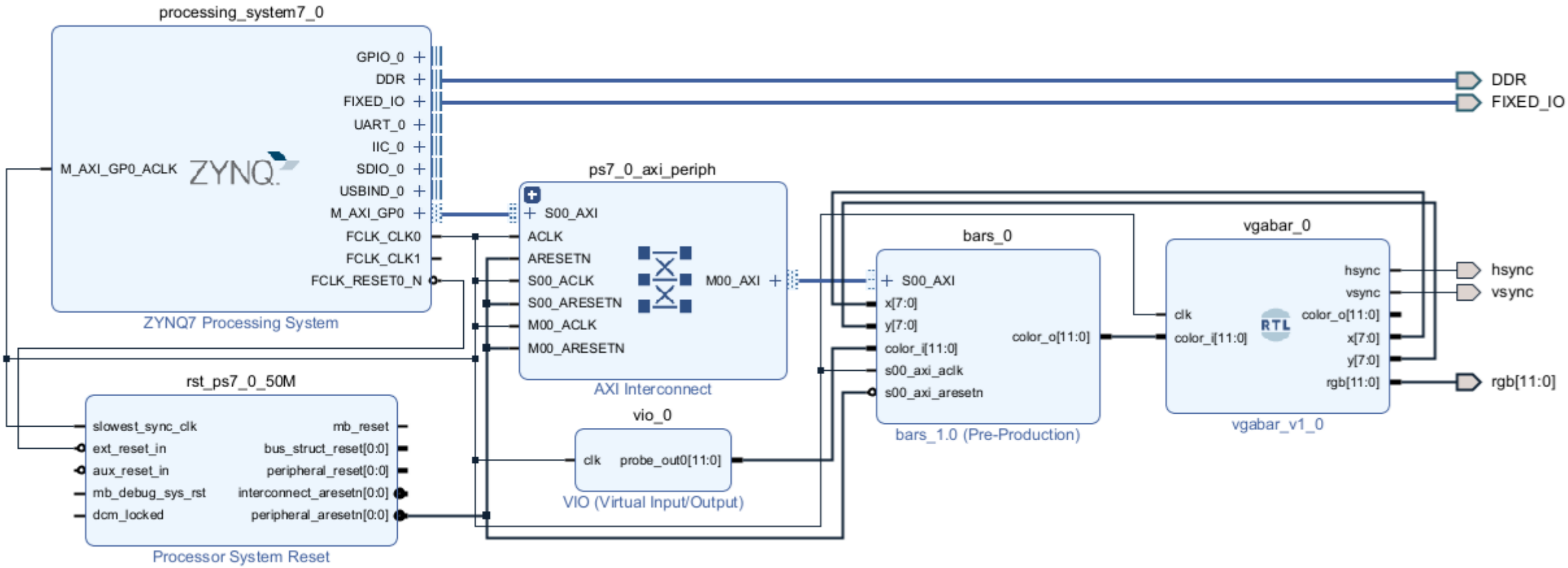
VIO parametri

- Določimo število navideznih vhodov in izhodov in za širino vsakega

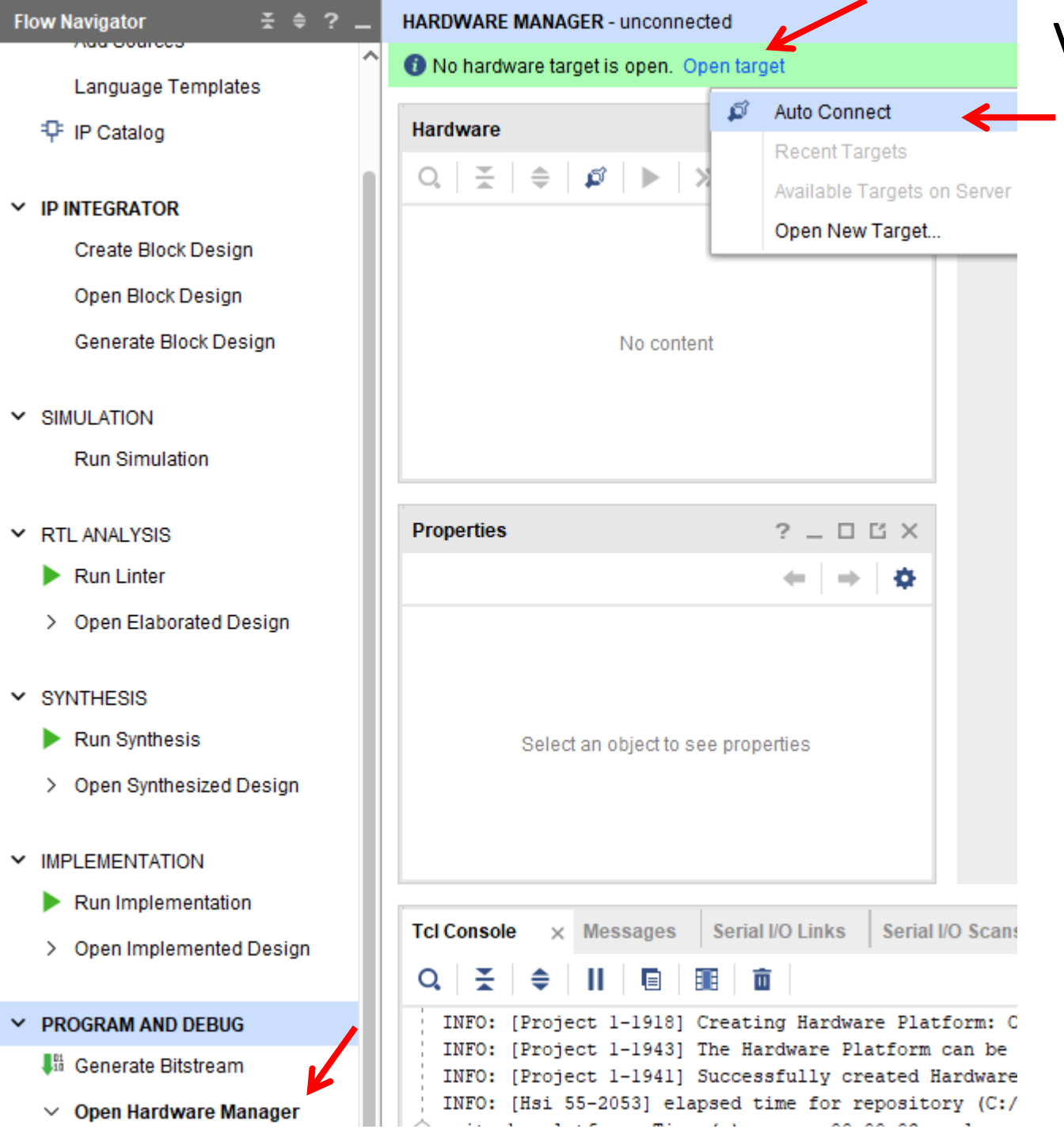


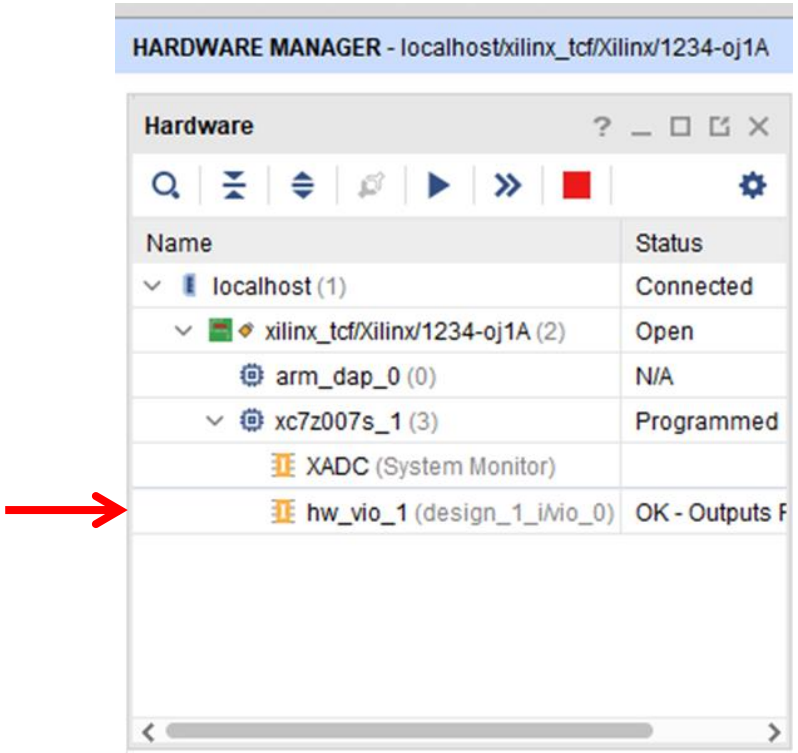


Npr: VIO za nastavljanje barve ozadja

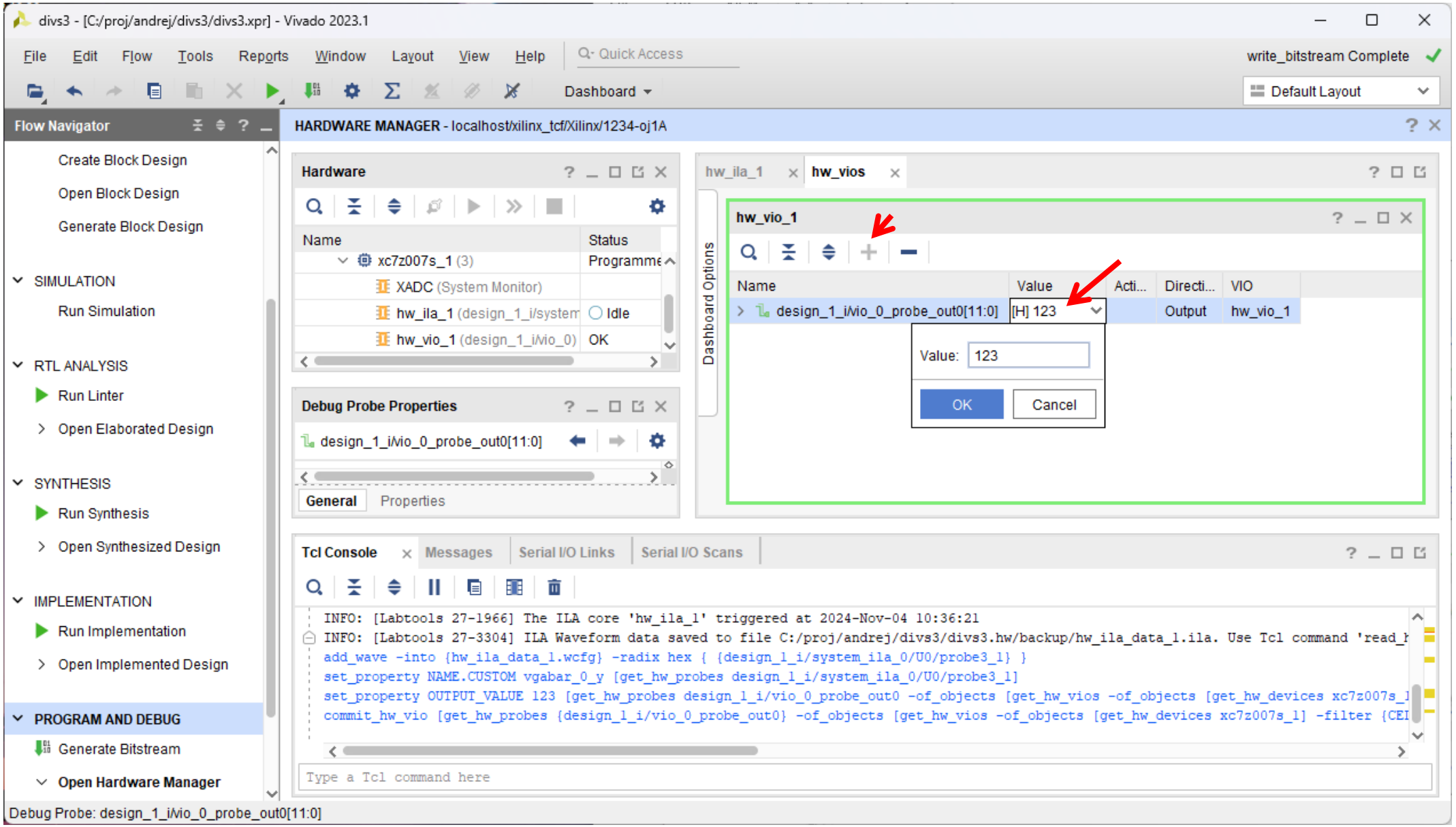


Vivado Hardware Manager



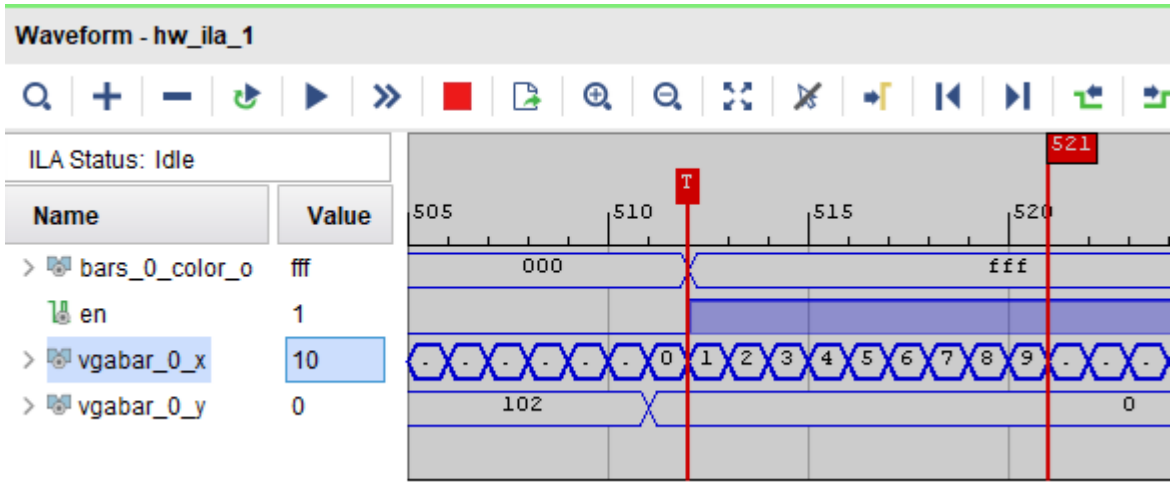


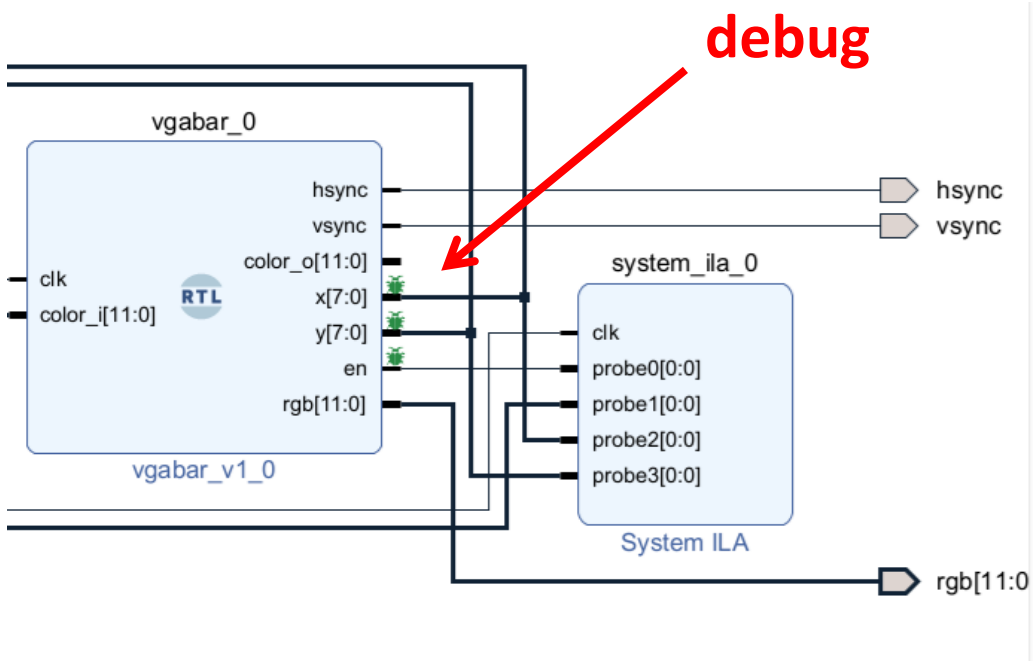
Nastavitev izhodne vrednosti VIO



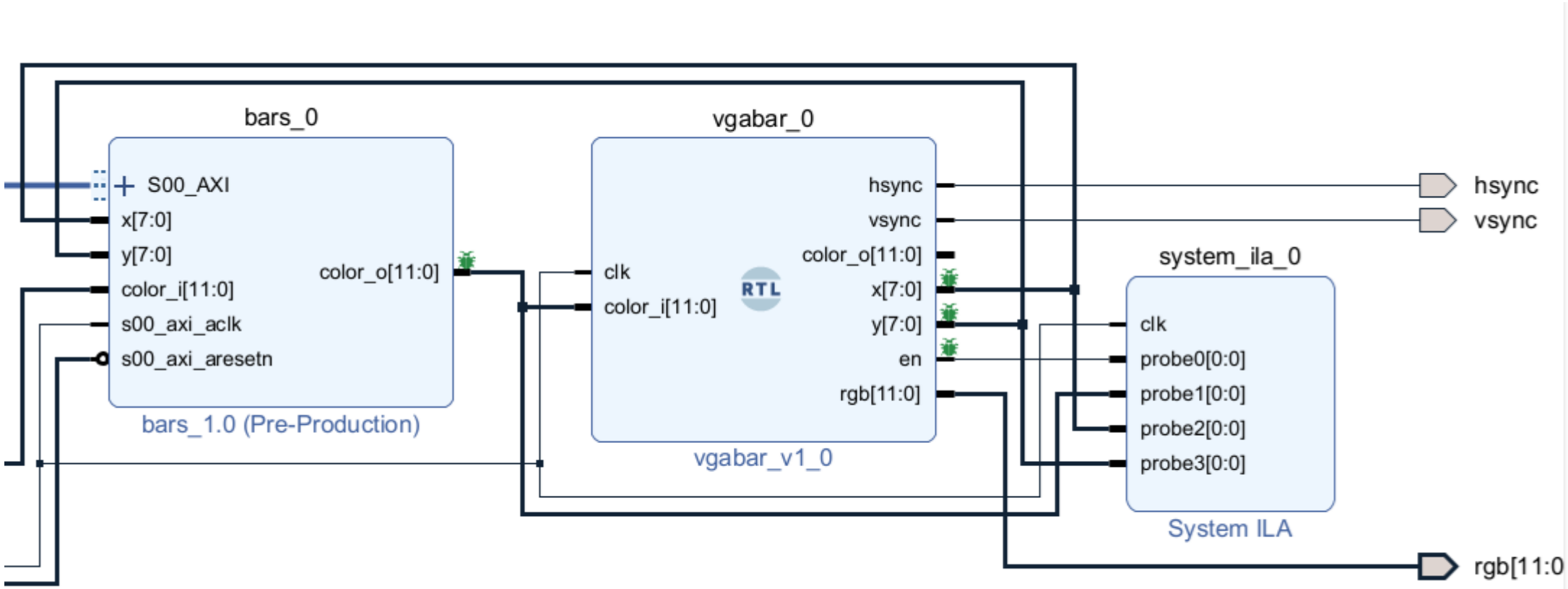
Vivado ILA – integrirani logični analizator

- Zajem hitrih signalov ob prožilnem pogoju, prenos podatkov po JTAG in prikaz v obliki časovnega diagrama (waveform)
- npr. zajem in prikaz 1k vzorcev z uro clk



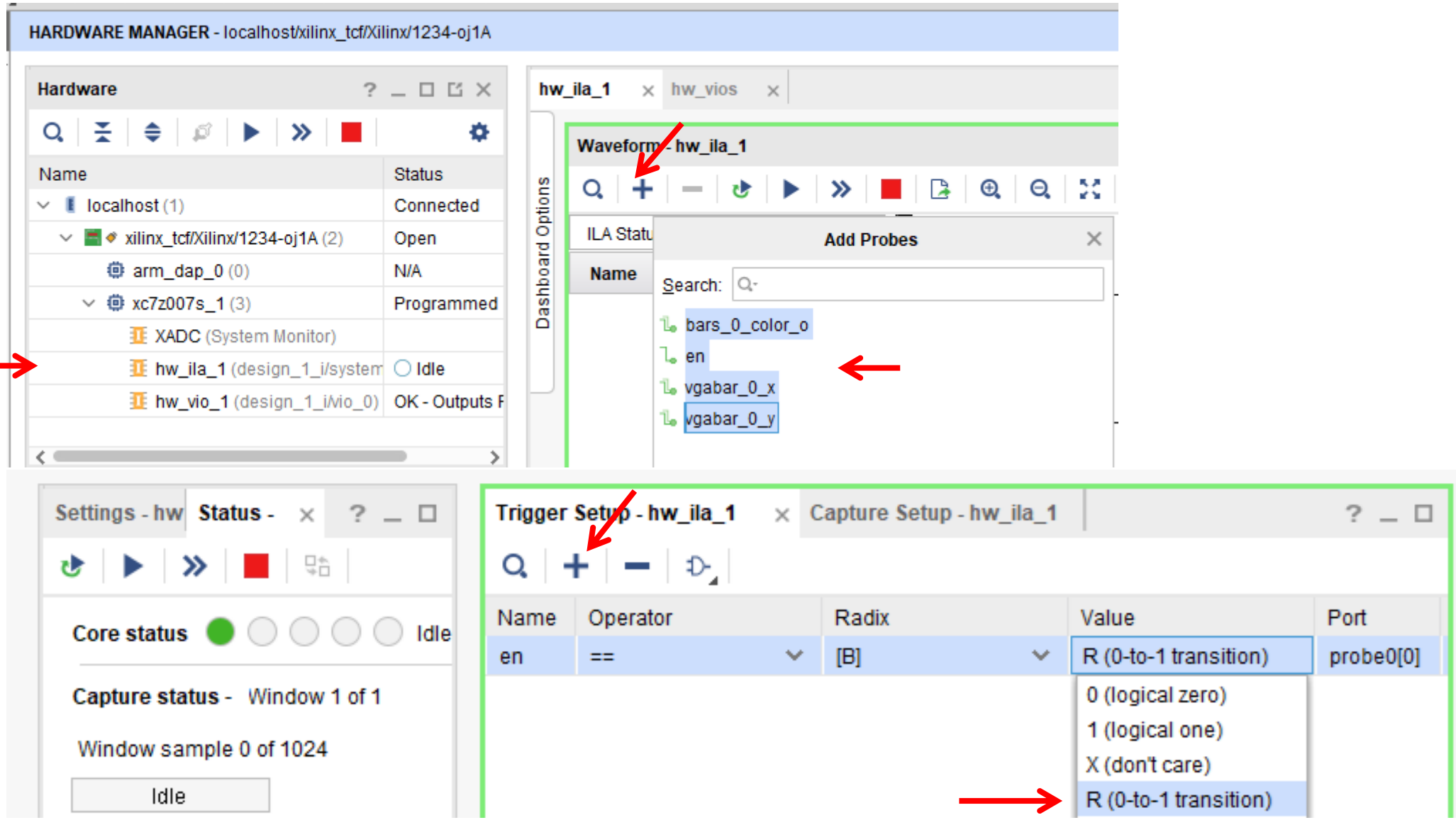


Debagiranje vgabar

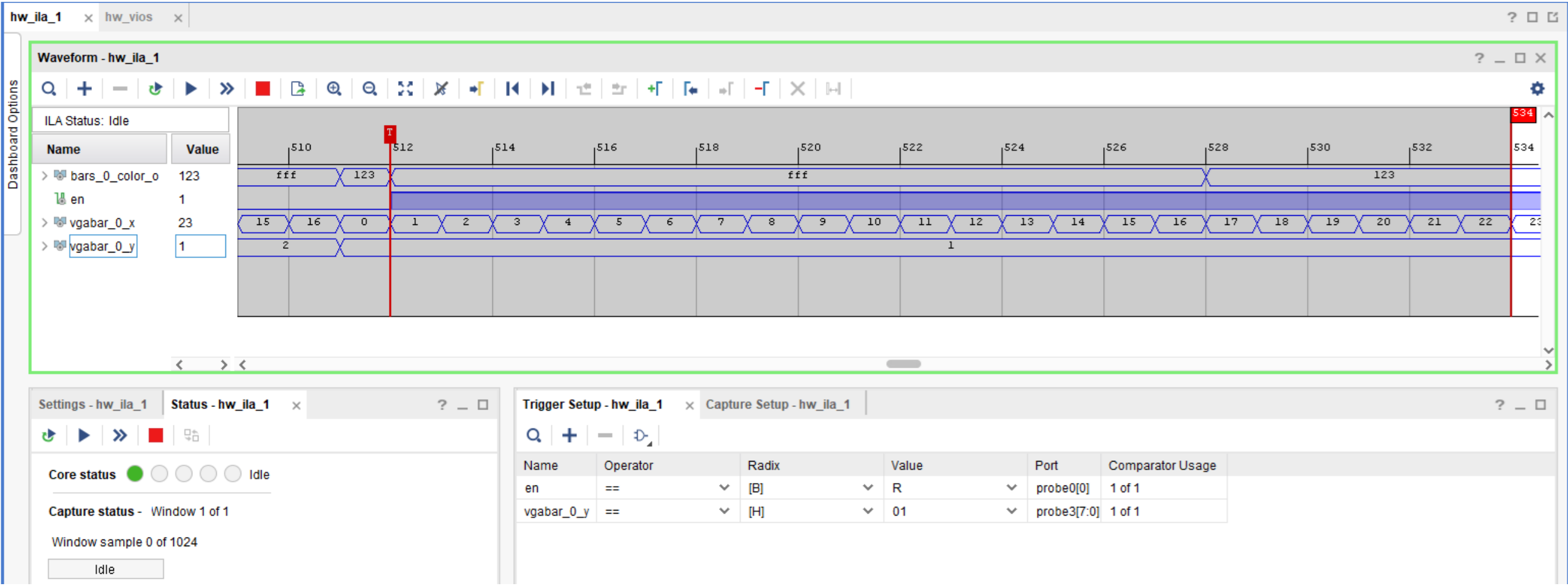


- v vgabar.vhd dodamo izhod en, ki je 1, ko smo znotraj okna s stolpci
- nastavimo debug na opazovane signale in prevedemo vezje

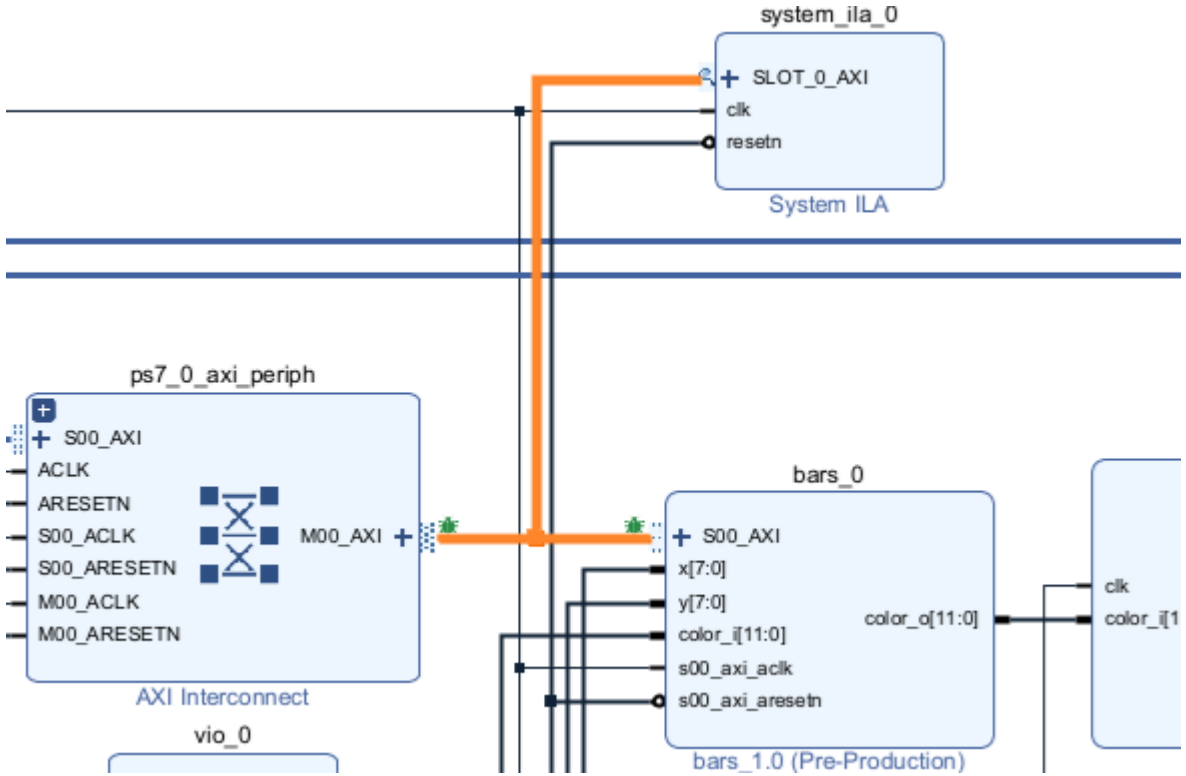
Dodajanje signalov in proženja



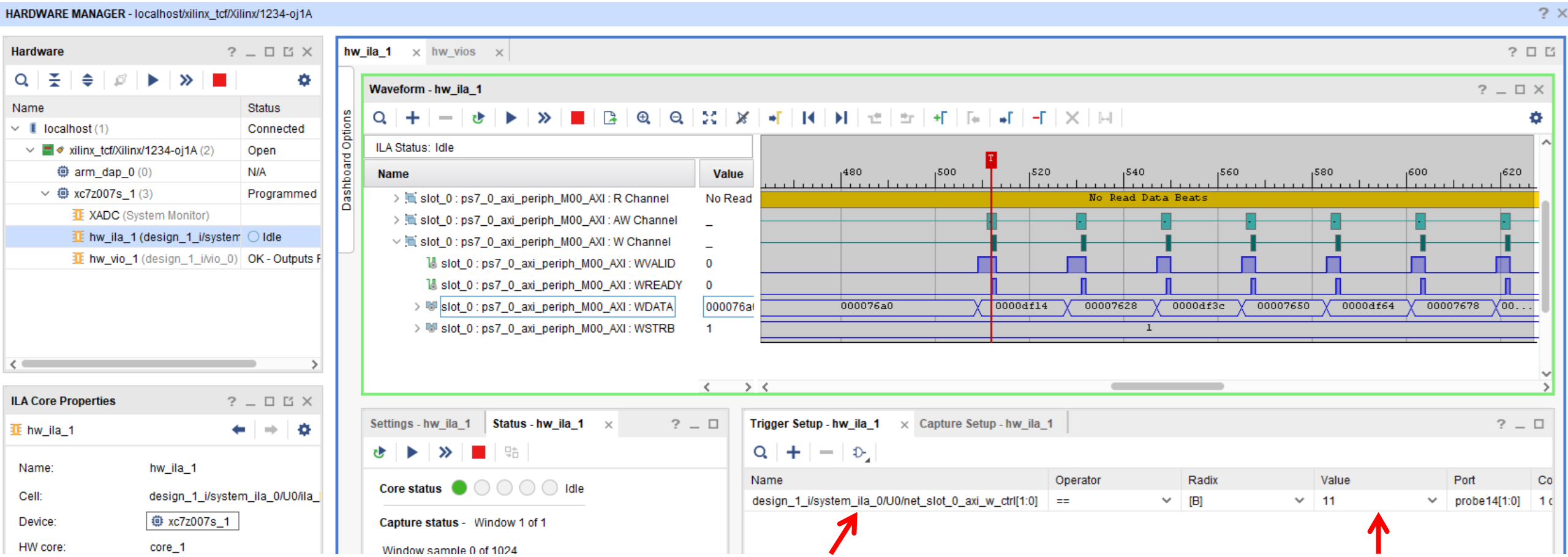
Pregled zajetih signalov



Opazovanje vodila AXI z ILA



Zajem transakcij na vodilu AXI



Vitis – poganjanje SW brez reprogramiranja FPGA