Laboratorij za načrtovanje integriranih vezij

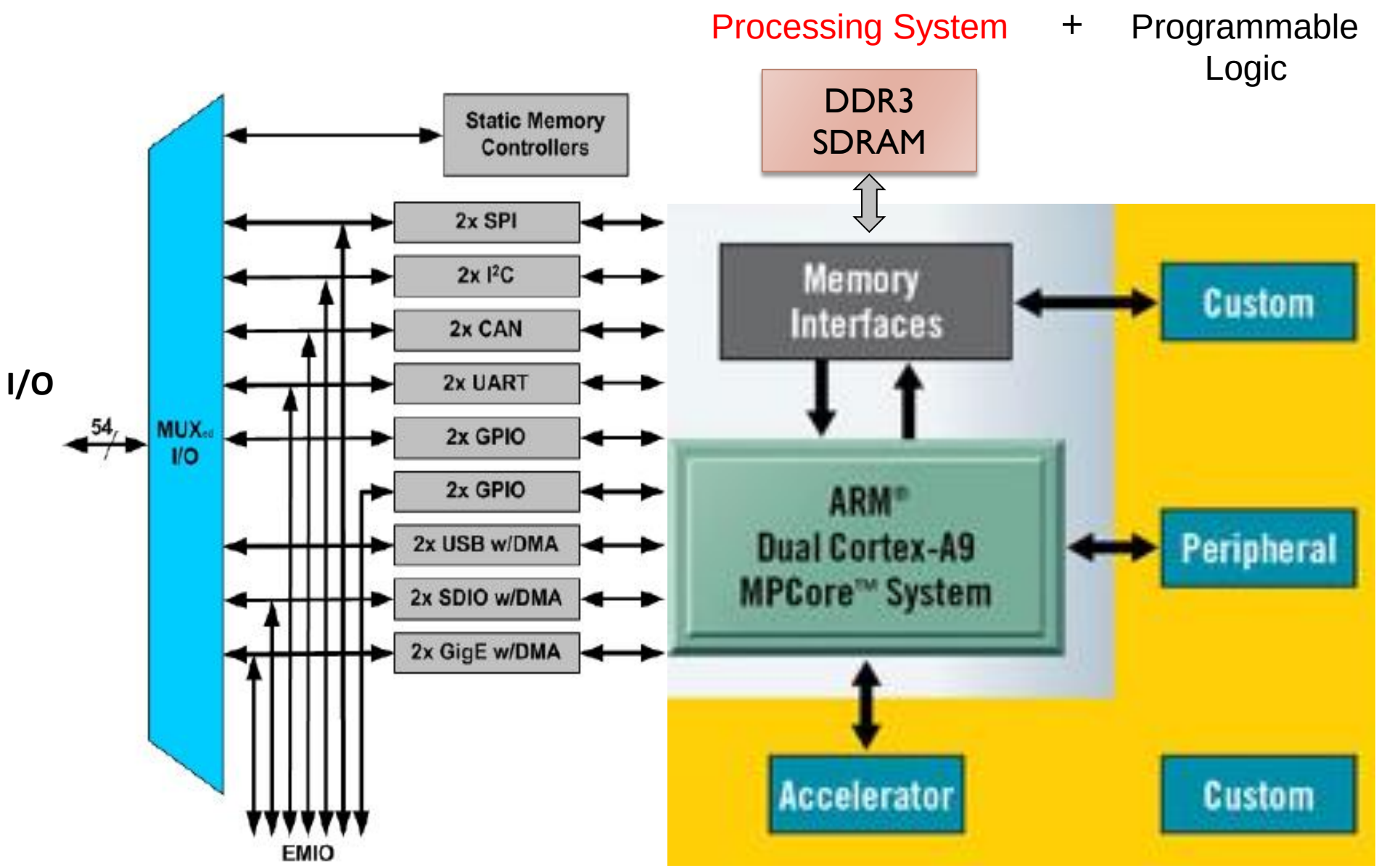
Univerza *v Ljubljani*
Fakulteta *za elektrotehniko*

Uvod v laboratorijske vaje

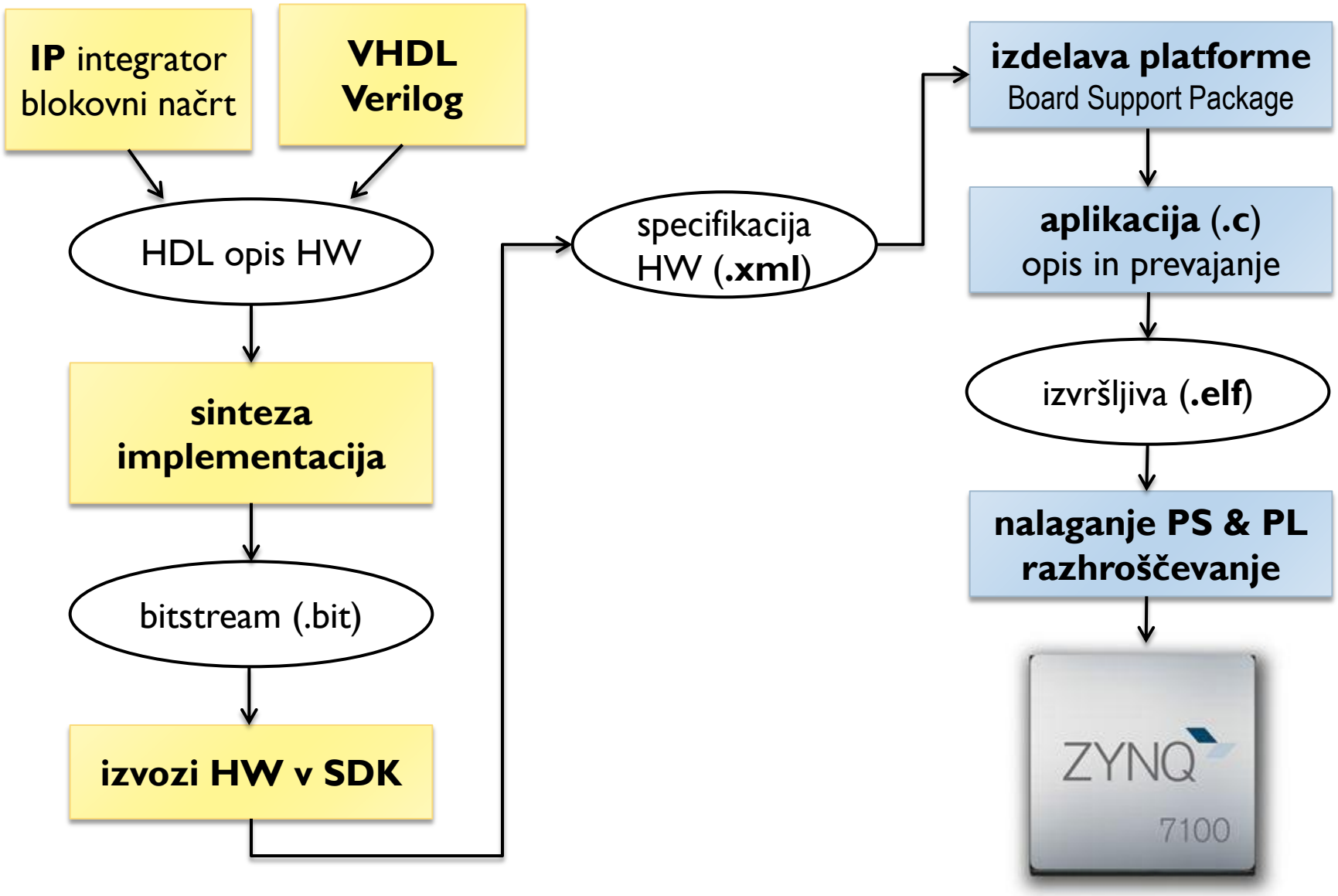
Digitalna integrirana vezja in sistemi

Literatura: A. Trost: Načrtovanje digitalnih vezij v jeziku VHDL, FE 2011
The Zynq Book, http://www.zynqbook.com/

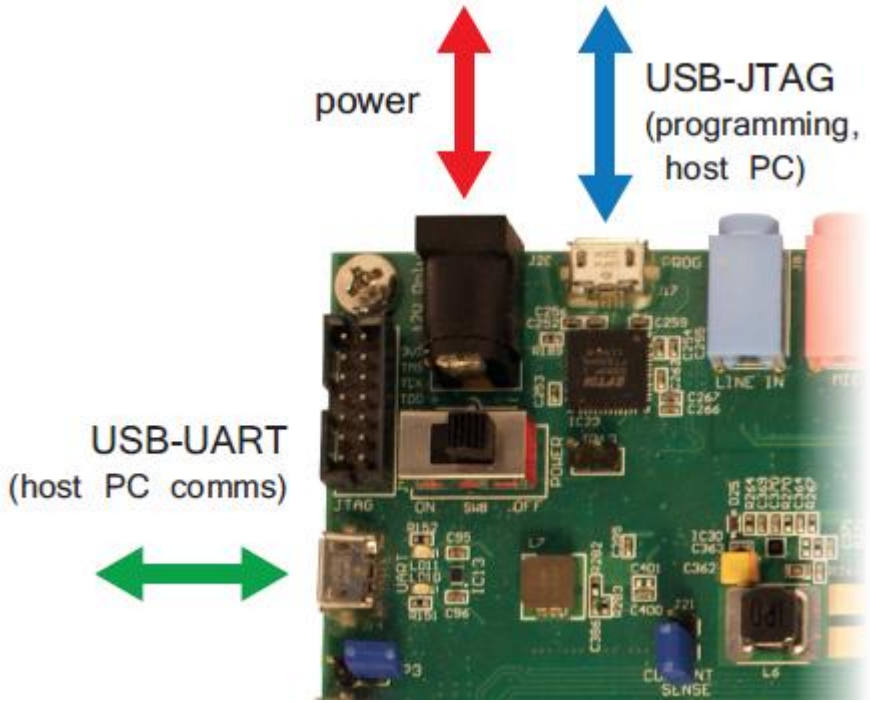
Programirljivi sistem na čipu Zynq-7000



Orodja: Vivado Software Development Kit



Razvojne plošče Zedboard in Red Pitaya



- XC7Z020-CLG484-1

  Artix-7 + 2xARM Cortex-A9

  13,300 rezin (Slice)

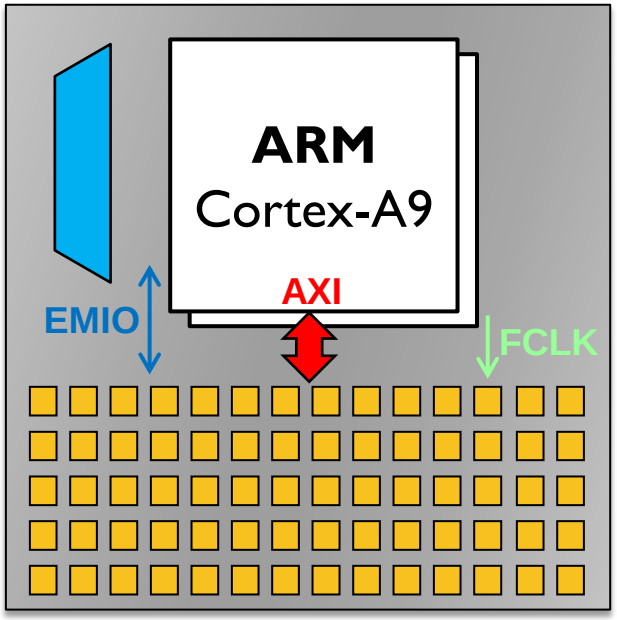
  220 blokov DSP48

  140 BRAM

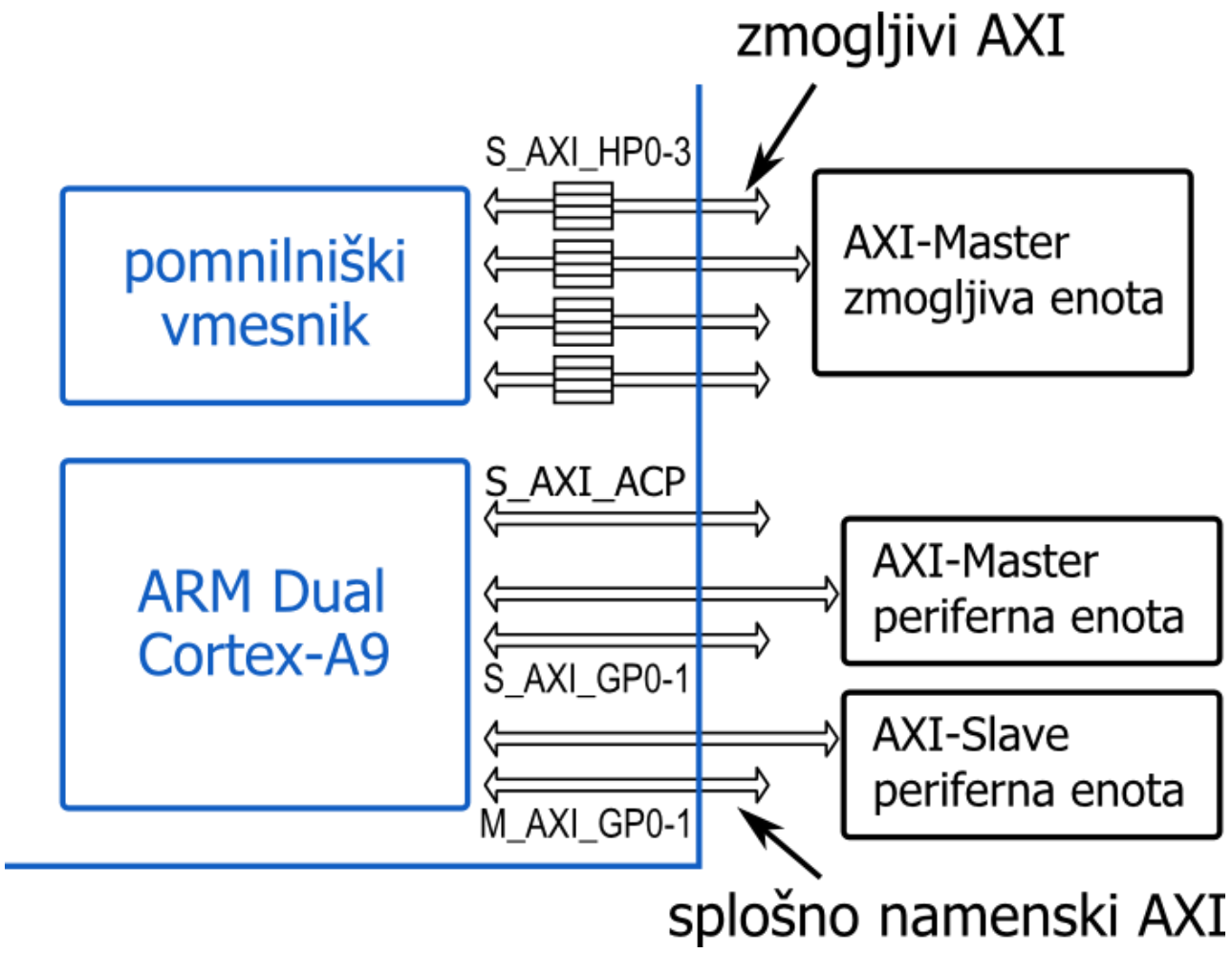
  XADC

Povezava ARM-FPGA

- vgrajene periferne enote (EMIO)
- pomnilniško preslikani vmesniki
  - Zynq uporablja AXI4 protokol in vmesnike
  - sistem nadrejenih enot (master-slave)

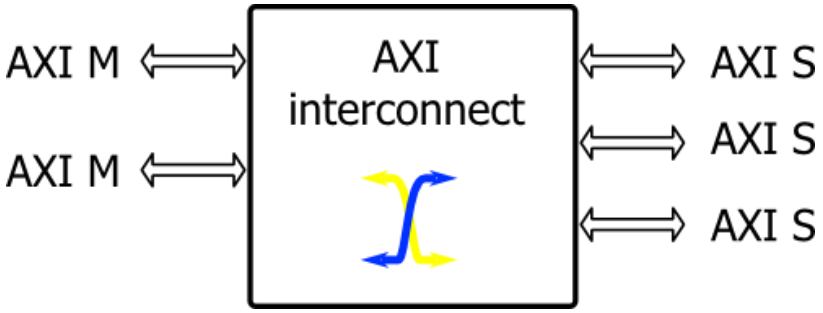


Vmesniki AXI na procesorskem sistemu



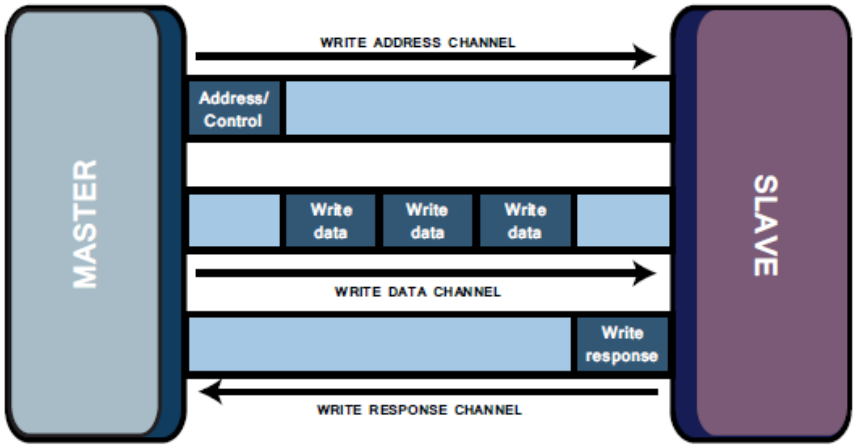
AXI4 (Advanced eXtensible Interface)

- pomnilniško preslikan vmesnik, preko AXI interconnect
  - AXI4 (full)
    - zmogljiv, kompleksen
    - do 256 podatkov/prenos
  - AXI4-Lite
    - manj signalov, enostavnejši
    - 1 podatek/prenos

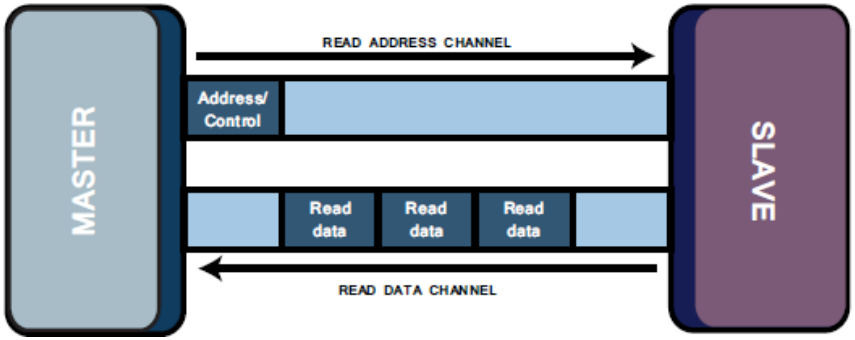


- pretočni vmesnik
  - AXI4-Stream
    - pretočni protokol brez naslovov

Vmesnik AXI4



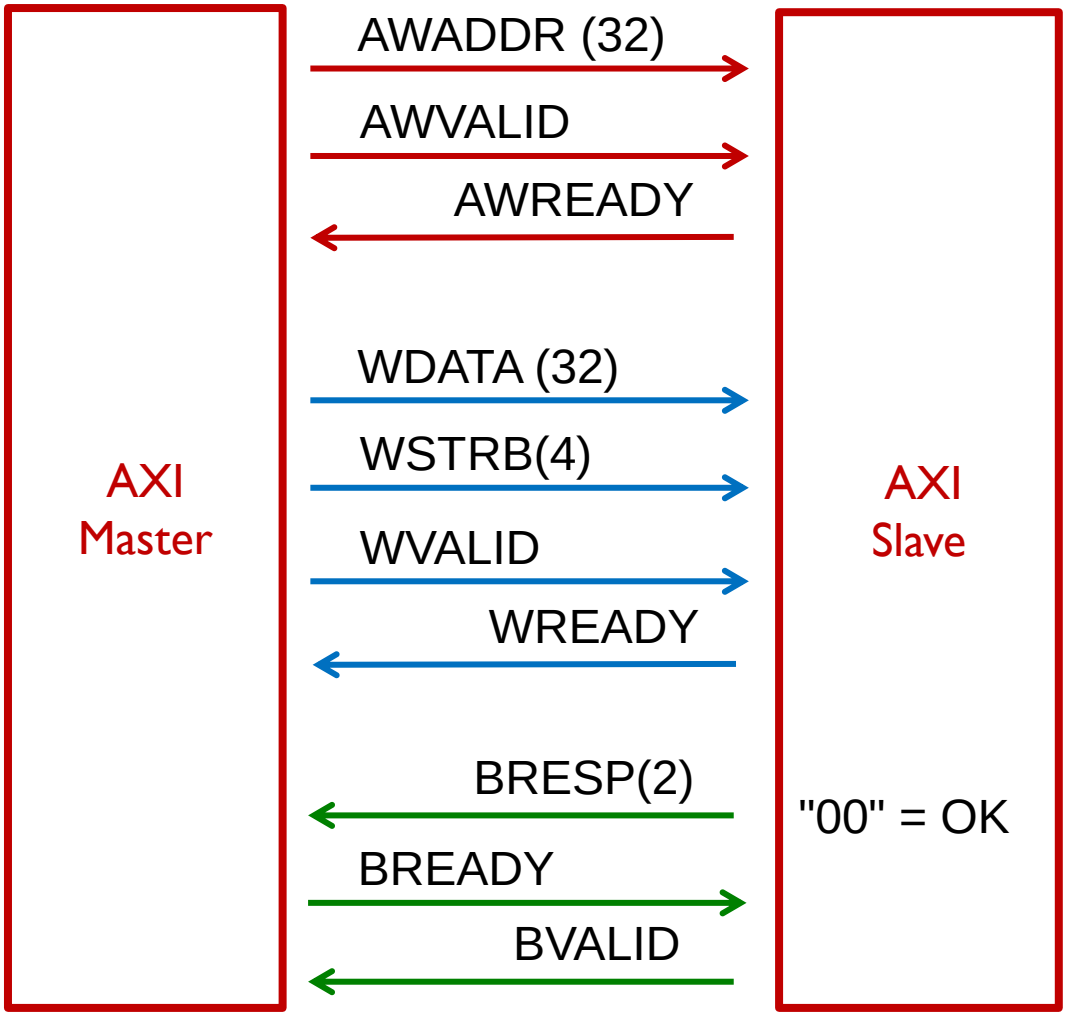
- pisanje podatkov
  - ločena kanala za prenos naslova in podatka
  - potrditveni kanal



- branje podatkov
  - kanala za naslov in podatke

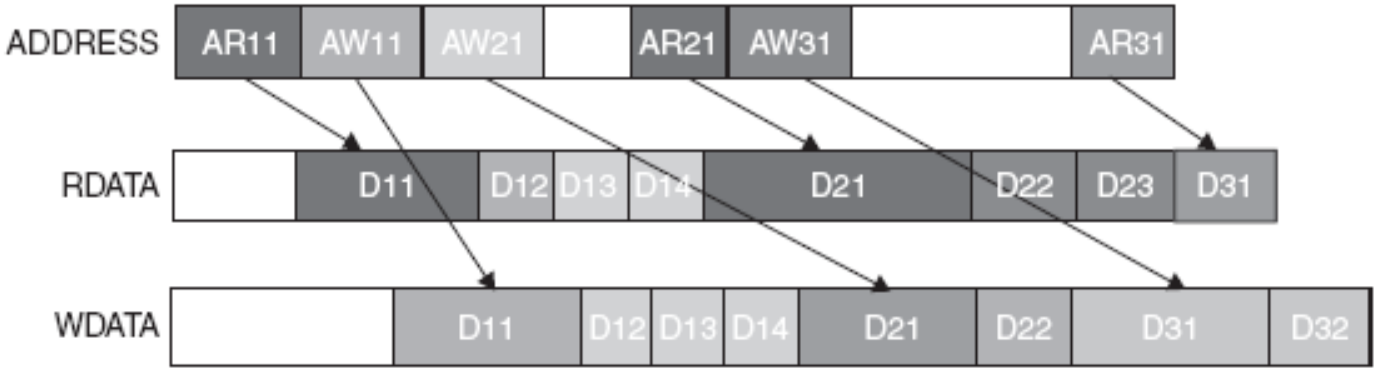
Signali…

- pisanje podatkov AXI4-Lite

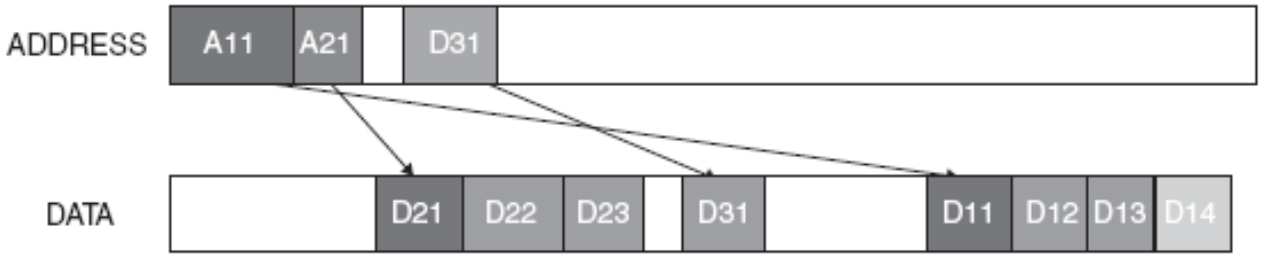


Paketni prenos AXI4

- sočasno branje in pisanje



- poljuben vrstni red zaključkov
  - hitre podrejene enote zaključijo prej kot počasne enote



1. vaja: izdelava periferne enote

- AXI4-Lite vmesnik s 4 registri (parvmes_0)
- demonstracijski sistem, prenos in kvadriranje podatkov