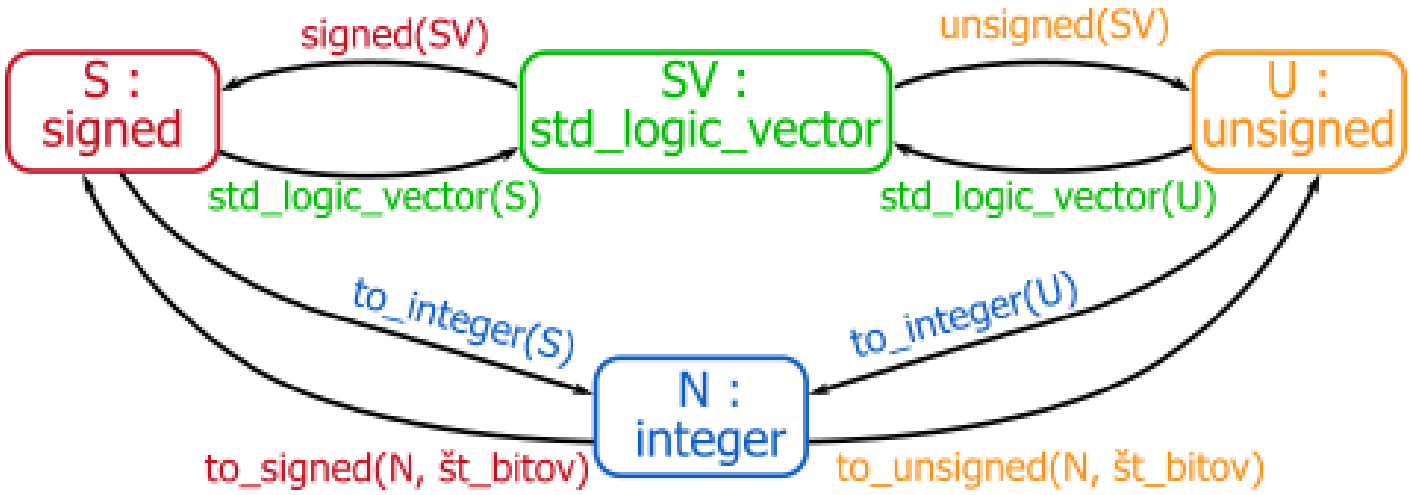
DIVS 2015, 1. vaja - povzetek

Digitalna integrirana vezja in sistemi

Kvadrirnik – VHDL koda

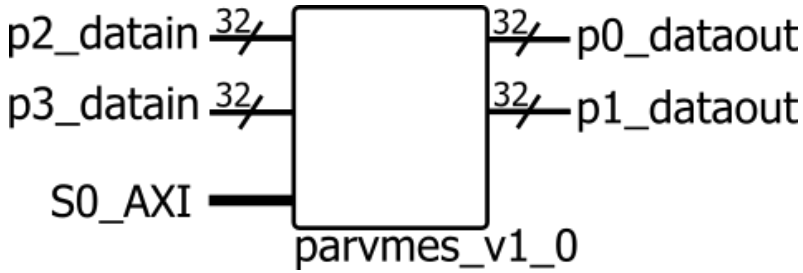
- pretvorba podatkovnih tipov



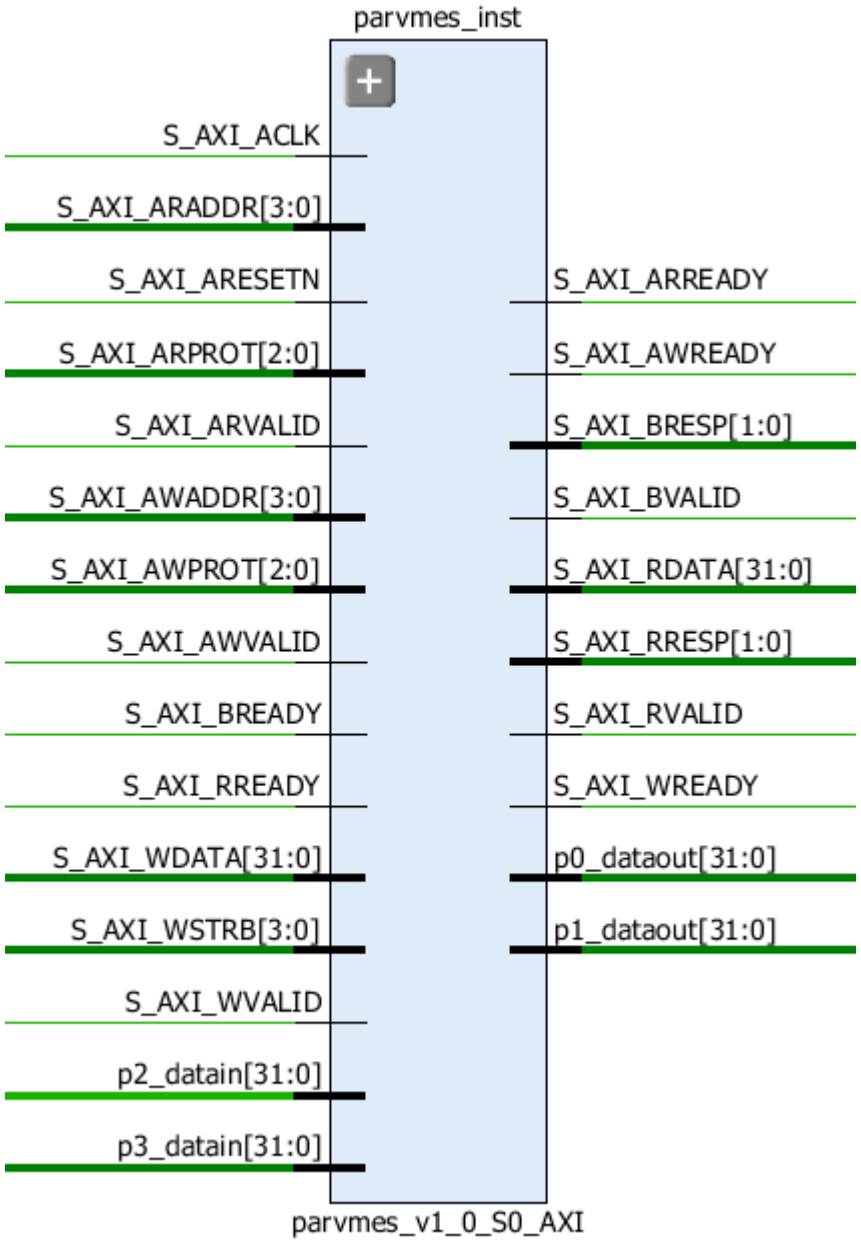

```
use IEEE.NUMERIC_STD.ALL;

a2 <= unsigned(a(7 downto 0)) * unsigned(a(7 downto 0));
```

Periferni vmesnik



- 4 registri, ki jih pišemo in beremo preko AXI Lite



Vključitev vmesnika v kvadrirnik

- deklaracija komponente

```
architecture arch_imp of kvadrat is
 component parvmes_v1_0_S0_AXI is
   generic ( C_S_AXI_DATA_WIDTH : integer := 32;
             C_S_AXI_ADDR_WIDTH : integer := 4 );
   port ( ... );
 end component;
begin
```

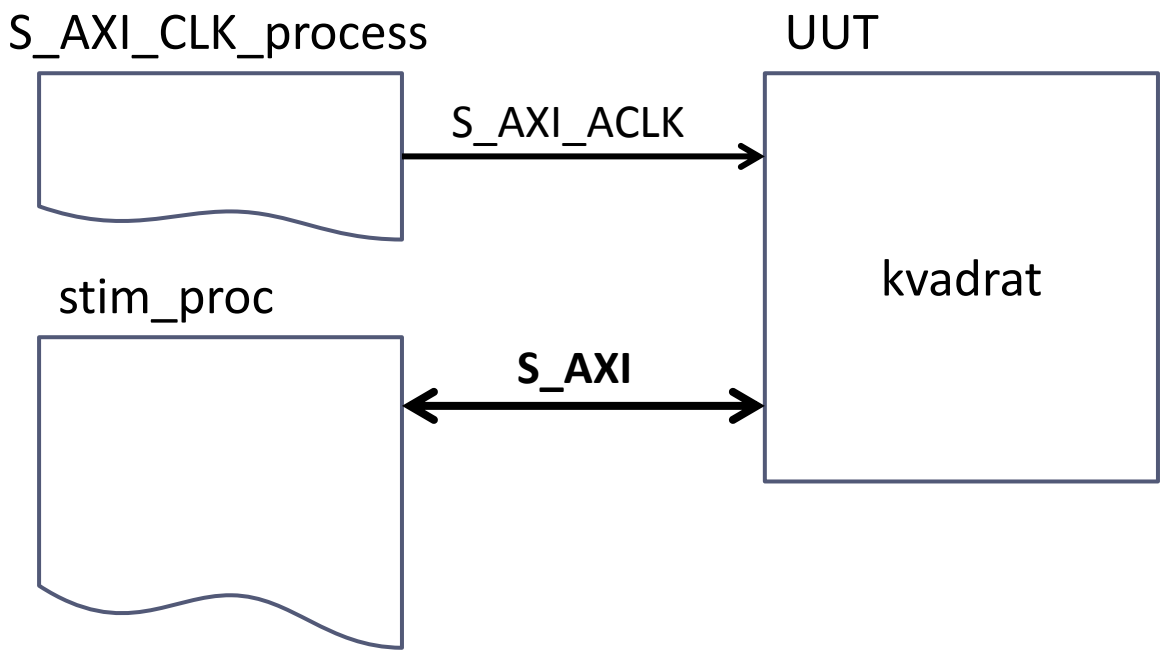
- povezava komponente

```
parvmes_inst : parvmes_v1_0_S0_AXI
  port map (p0_dataout => a,
            S_AXI_ACLK => s0_axi_aclk,
            ... );
```

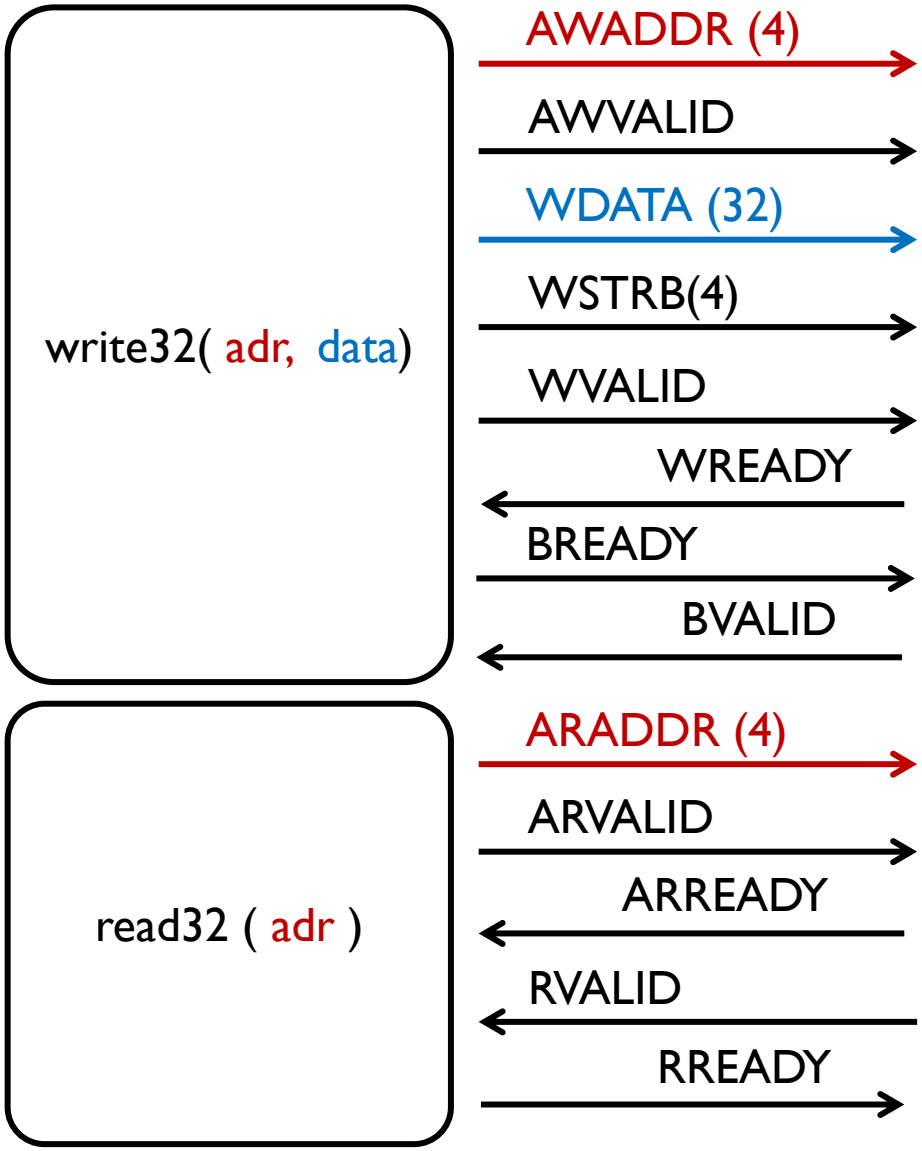
priključki komponente

zunanji priključki ali notranji signali

Simulacija s testno strukturo

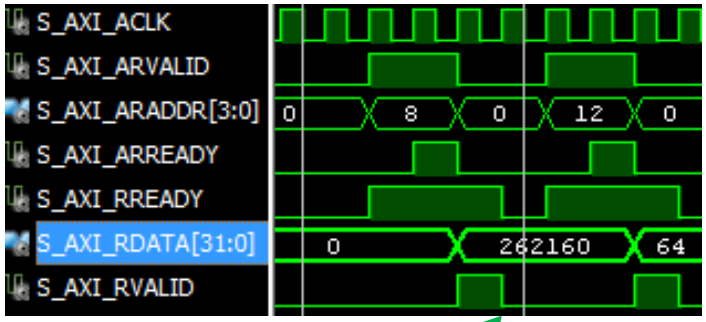


Proceduri za pisanje in branje AXI



VHDL:

```
write32(0, 2); -- p0_dataout
write32(4, 4); -- p1_dataout
read32(8);  -- a2_b2
read32(12); -- a2*b2
```



RDATA ob RVALID

Nadalnje delo

- Dopolni testno strukturo (stim_proc) z več testnimi vektorji
  - preizkus delovanja kvadrirnika pri mejnih vrednostih
- Sprememba algoritma in ali vmesnika
- Kako izdelamo nov/drugačen periferni vmesnik ?

1. Tools > Create and Package new IP
2. Create a new AXI 4 Peripheral
3. nastavi lastnosti :
4. Edit IP
5. popravi / dopolni kodo in dodaj priključke
6. preveri sintakso (sinteza)
7. Review and Package IP