



Laboratorij za načrtovanje integriranih vezij

Univerza *v Ljubljani*  
Fakulteta *za elektrotehniko*



1. stopnja UNI, 2. letnik

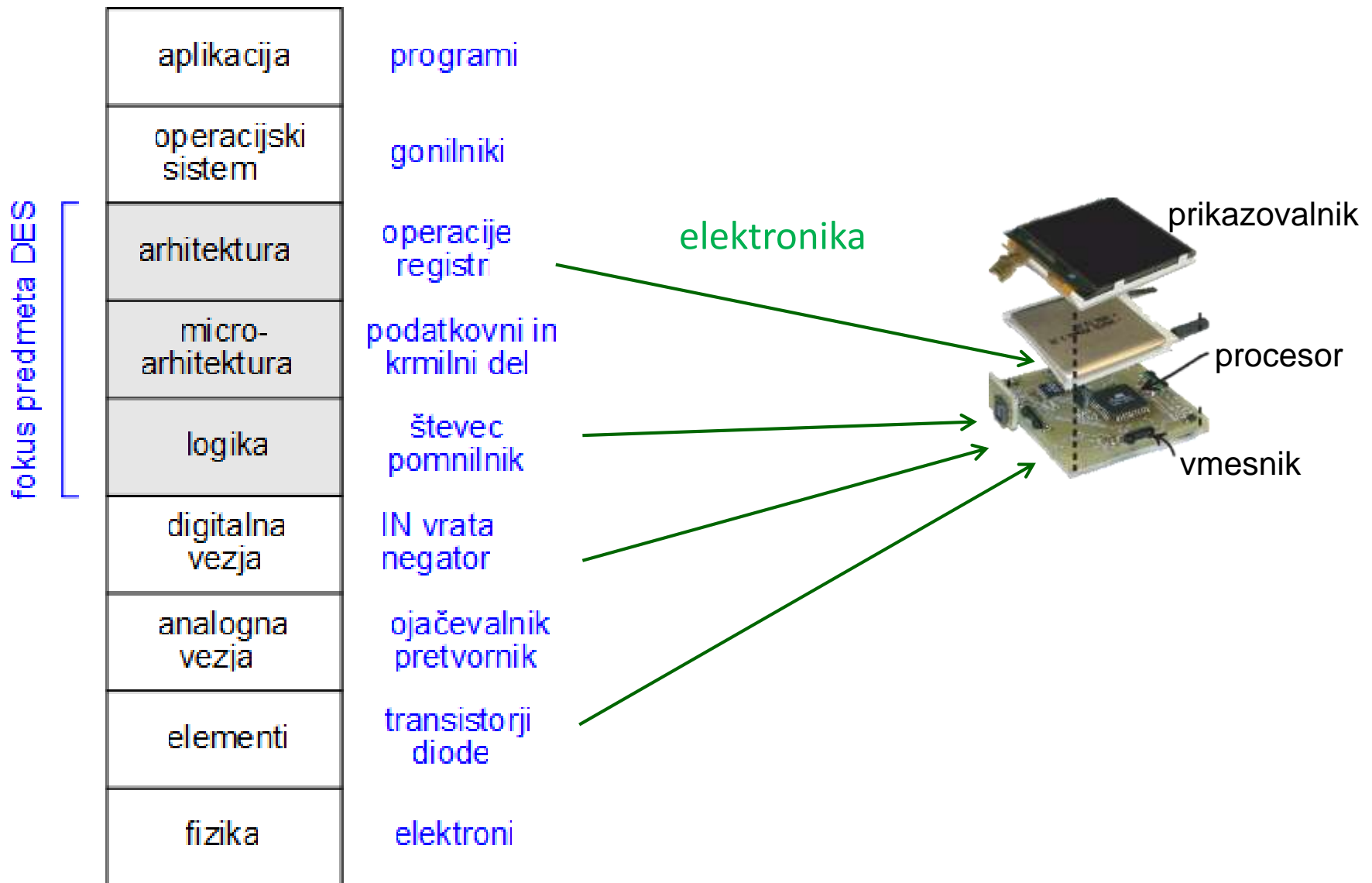
# Digitalni Elektronski Sistemi

Andrej Trost

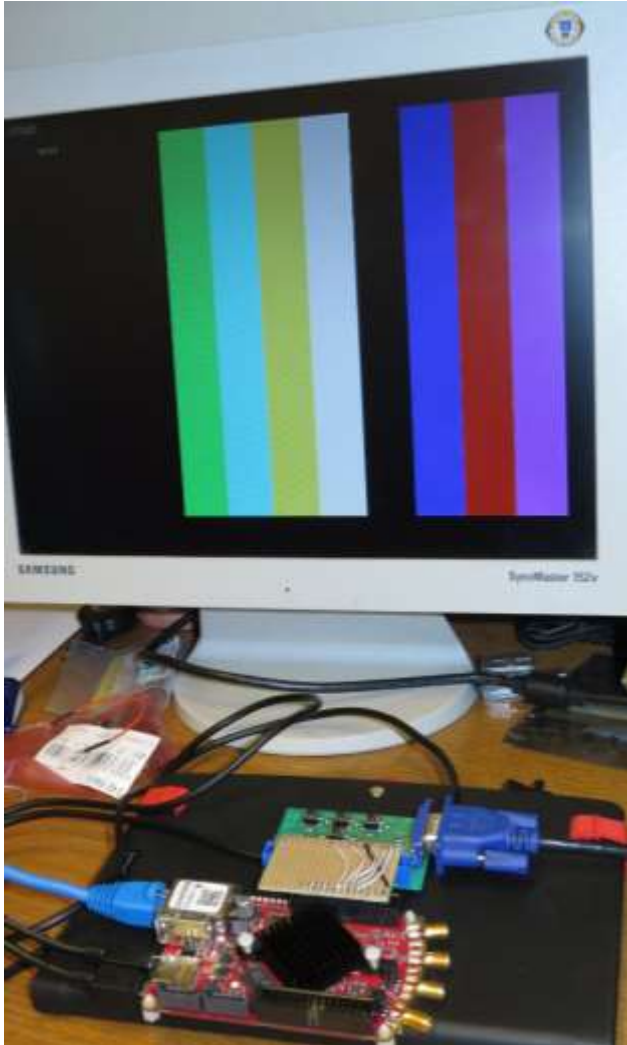
Literatura: A. Trost: Načrtovanje digitalnih vezij v jeziku VHDL, FE 2011

Spletna stran: <http://lniv.fe.uni-lj.si/des.html>

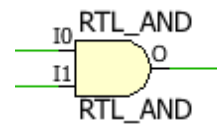
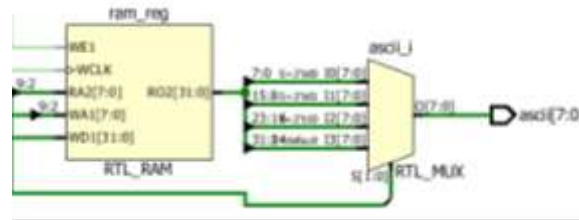
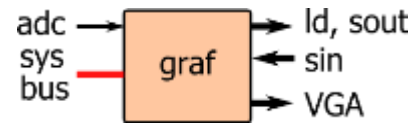
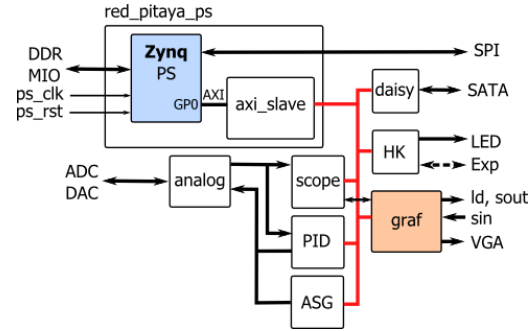
# Digitalni elektronski sistemi



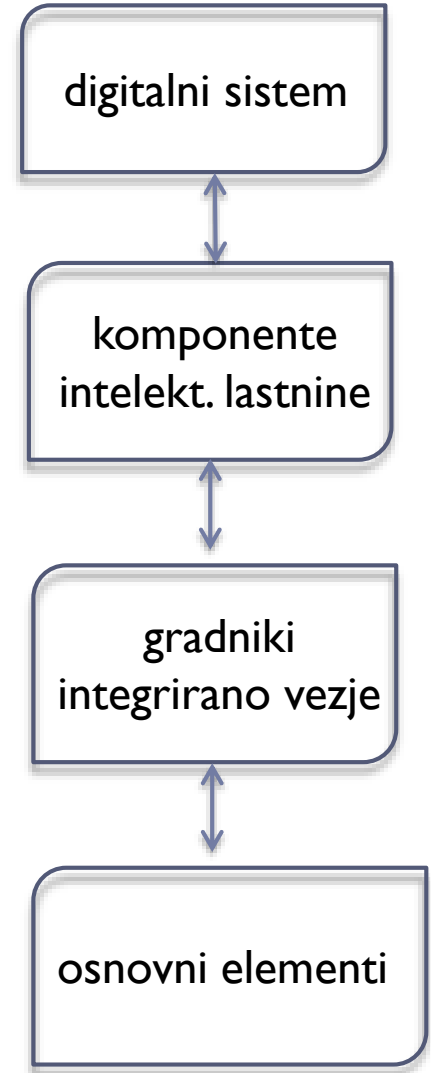
# Prototip vezja



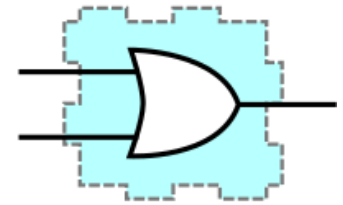
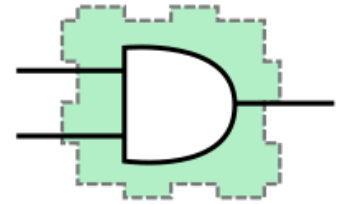
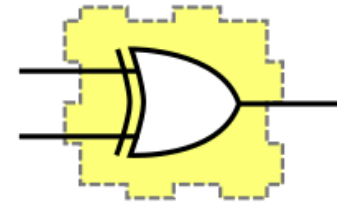
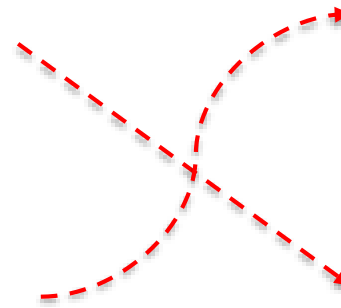
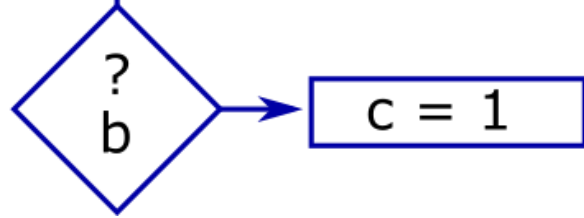
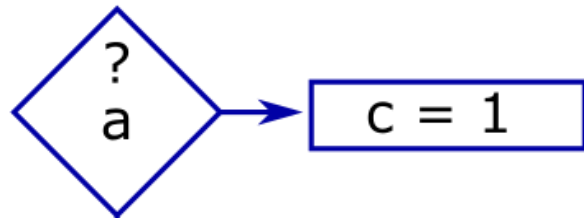
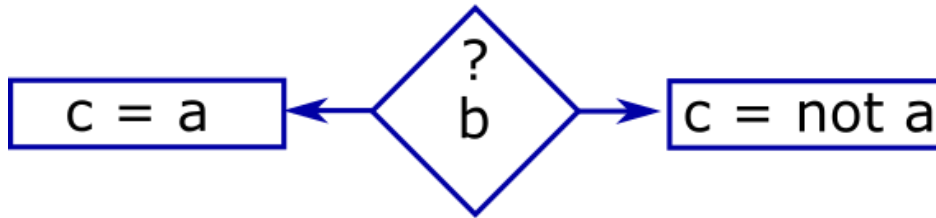
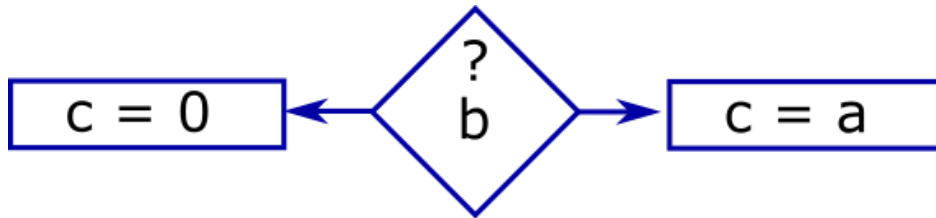
# Logični model



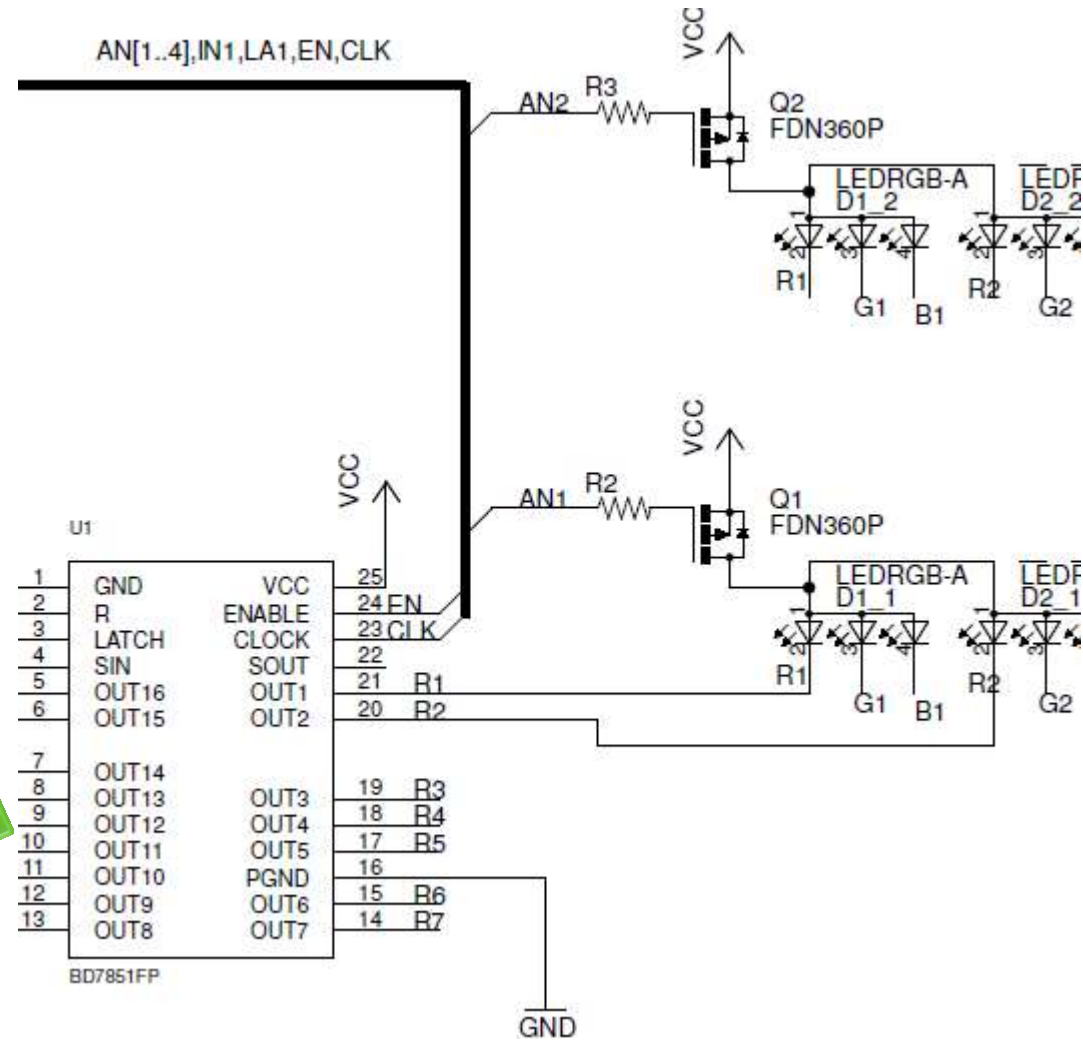
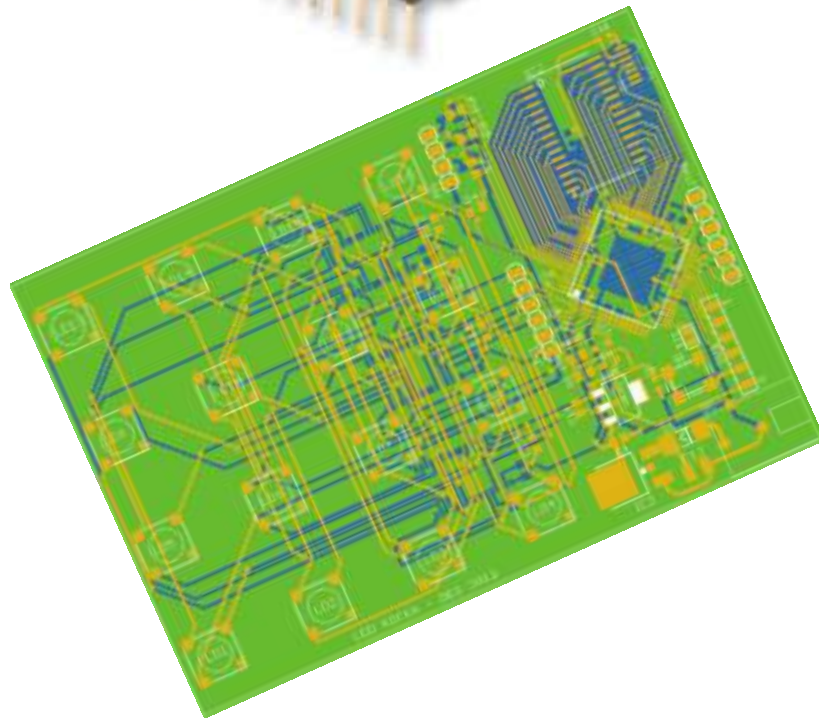
# Načrtovanje



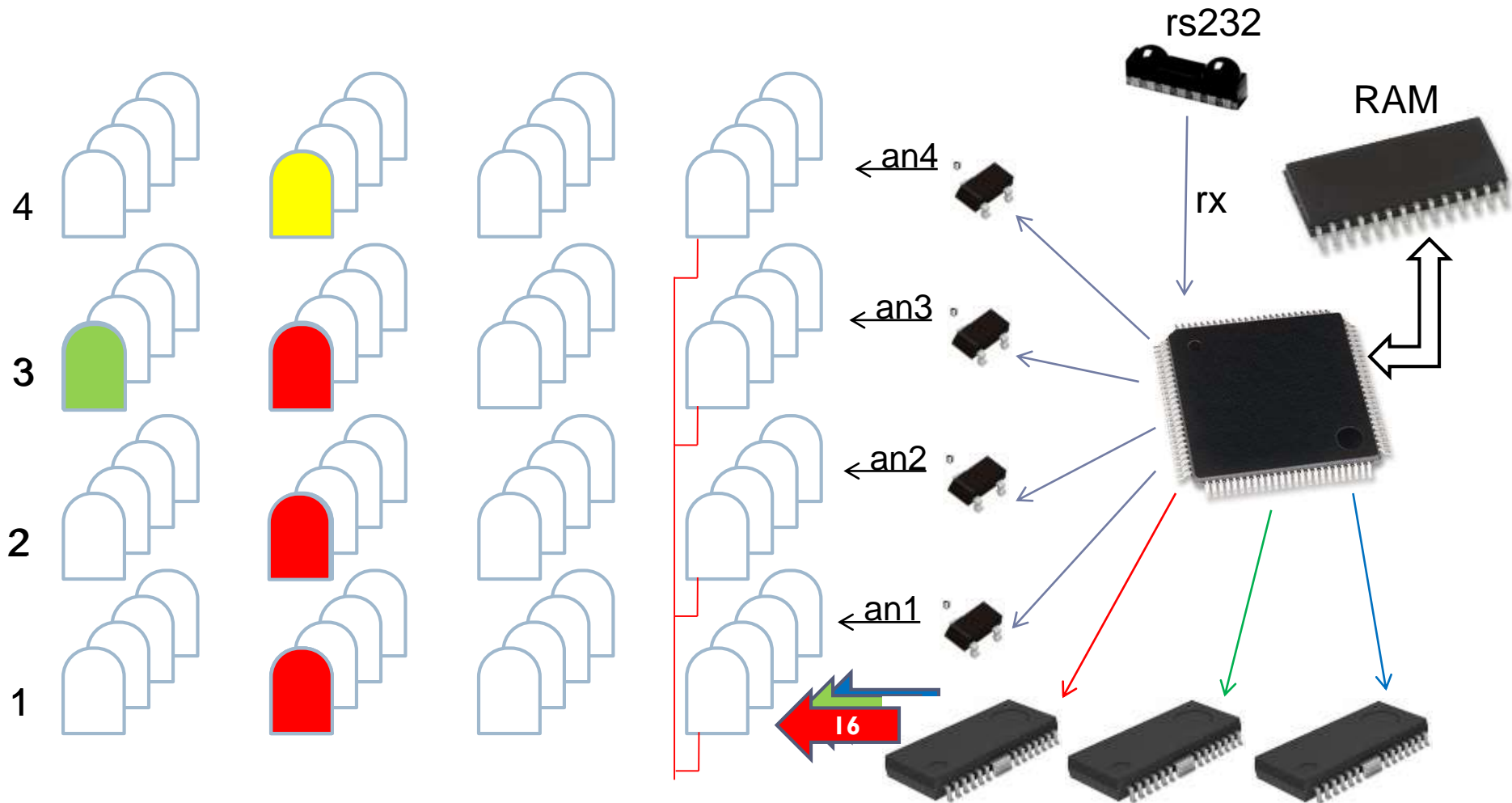
# Poveži diagram z logičnim gradnikom



# Svetleča kocka (2011/12)

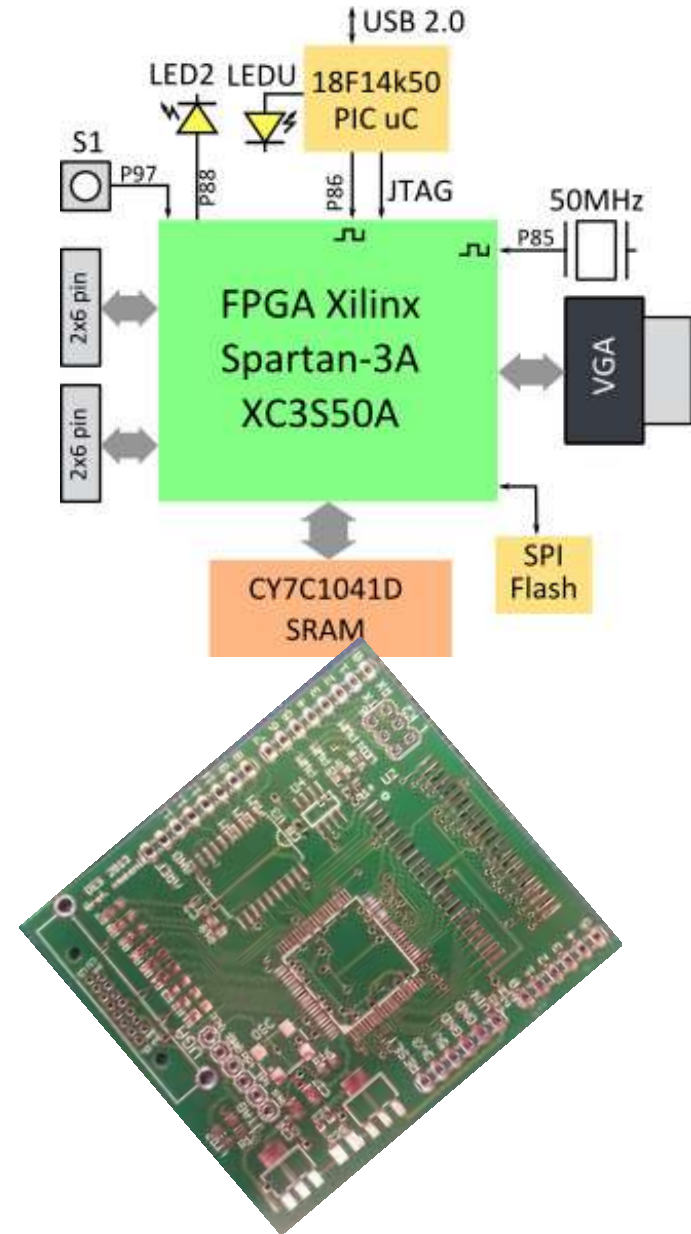
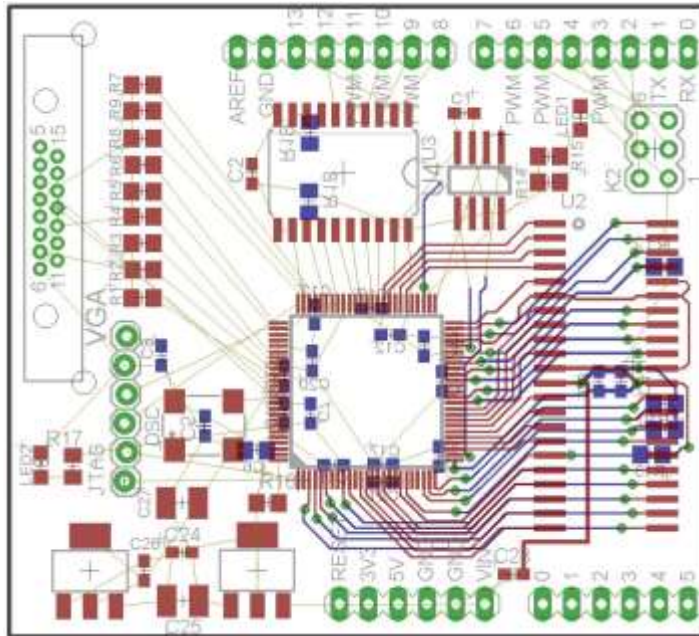
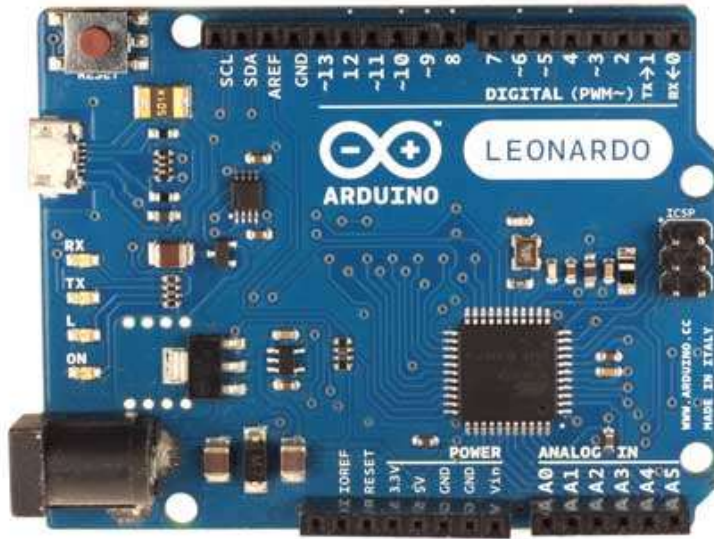


# Signali in krmiljenje kocke

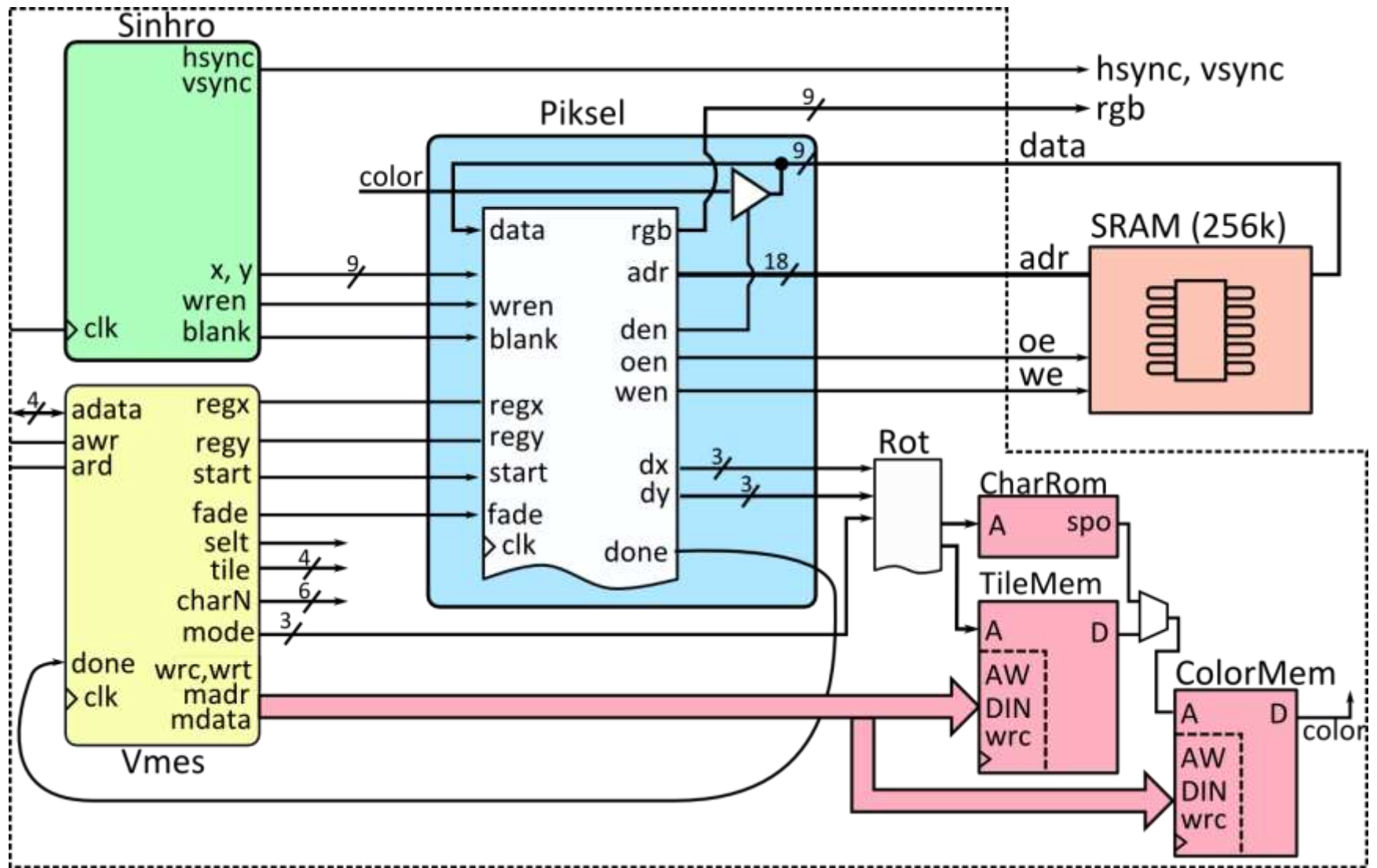




# Arduino grafični vmesnik (2012-13)



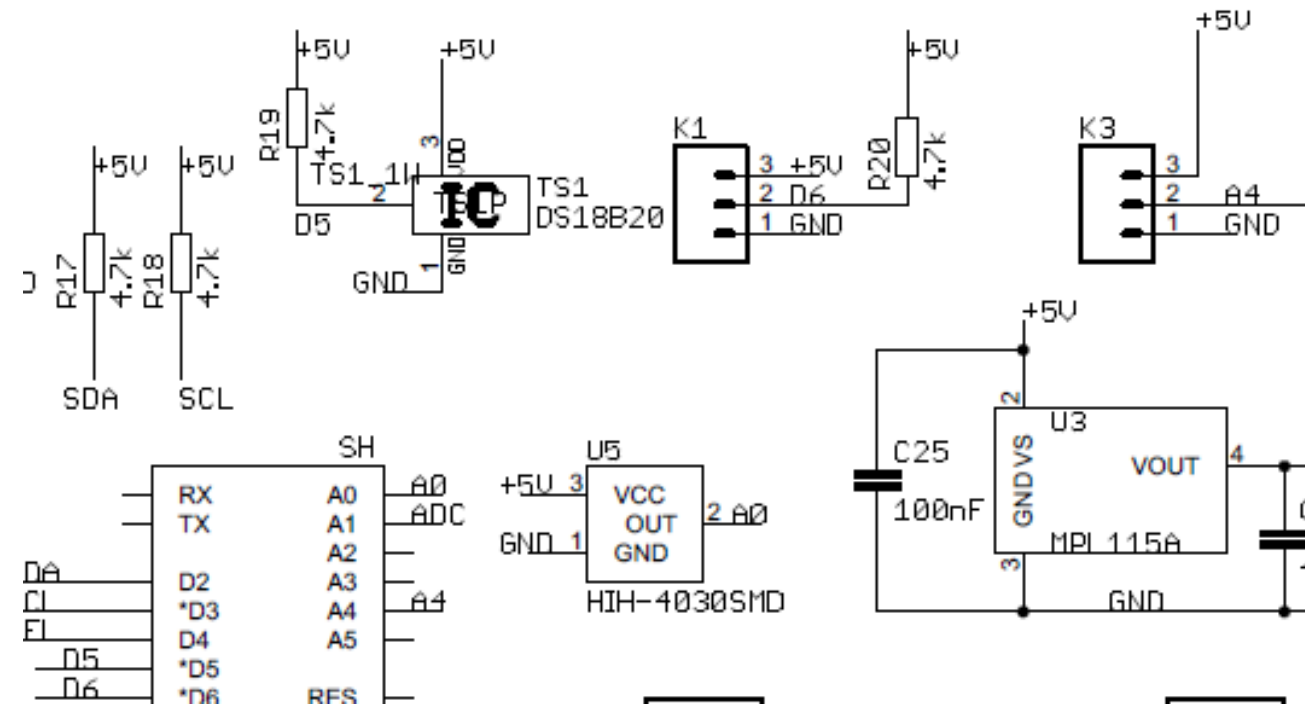
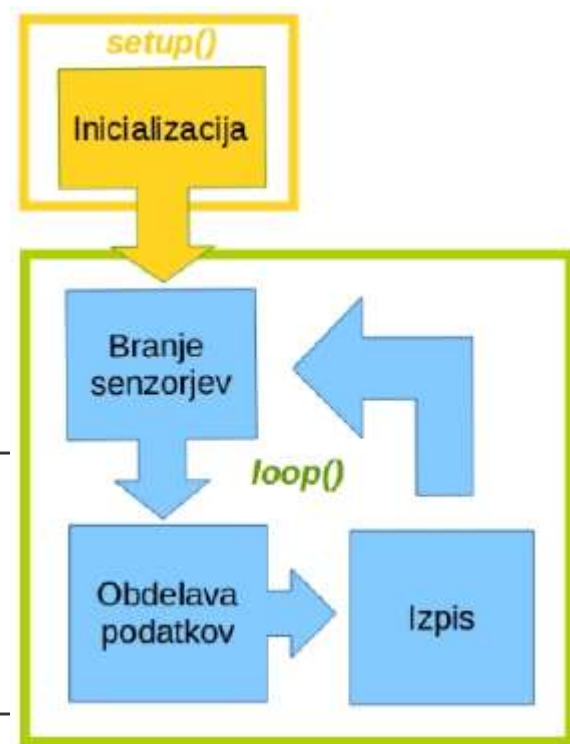
# Logična shema grafičnega vmesnika



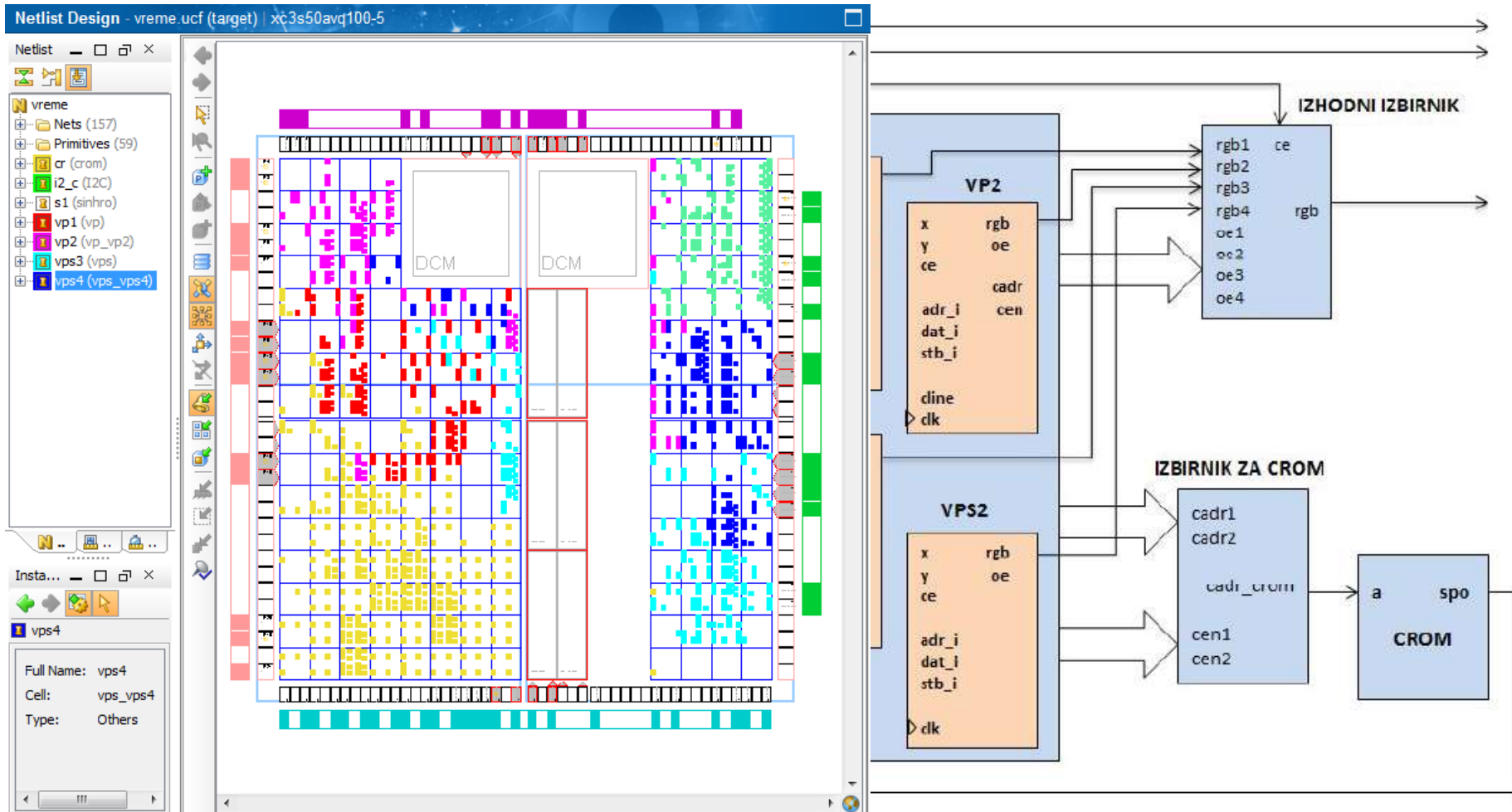


# Vremenska postaja (2013-14)

- ▶ temperatura DS18B20, 1wire
- ▶ vlaga HIH-5030, analogni (A0)
- ▶ tlak MPXA6115, analogni (A1)

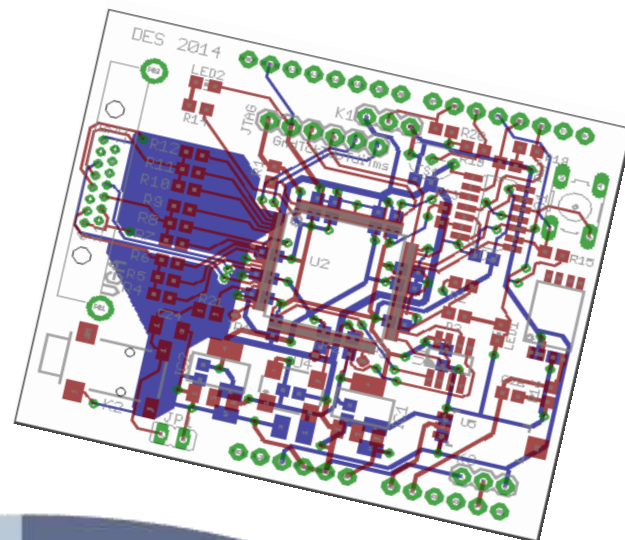


# Grafični prikaz podatkov - FPGA

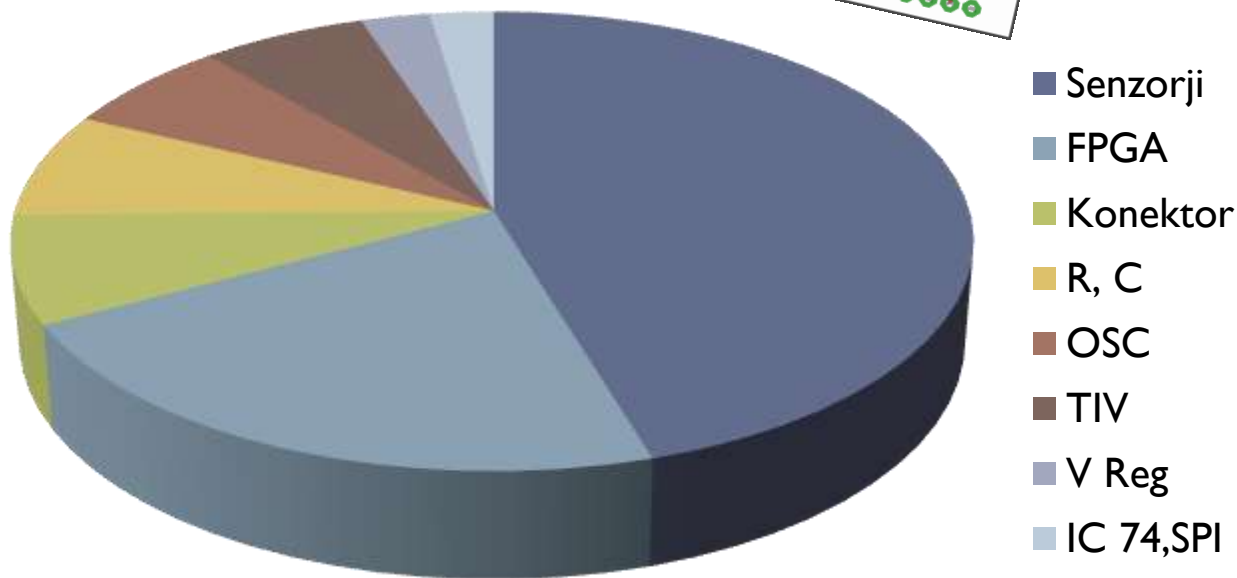


# Cena prototipne vremenske postaje

- ▶ Arduino Leonardo 22€
- ▶ Grafični vmesnik 46€

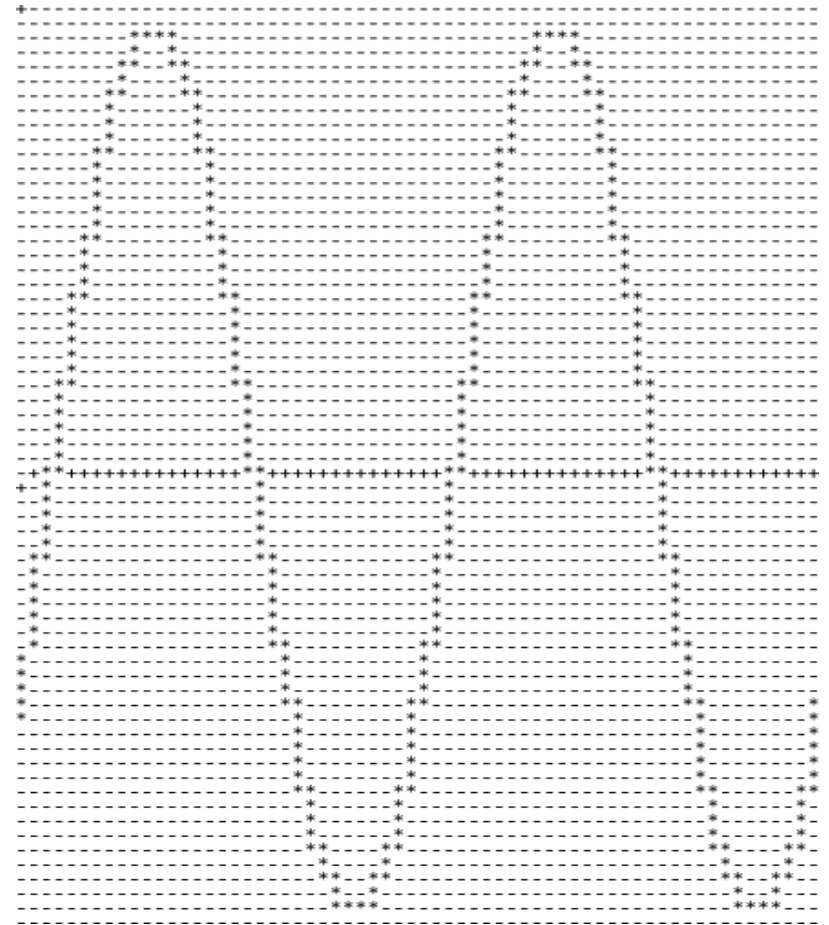
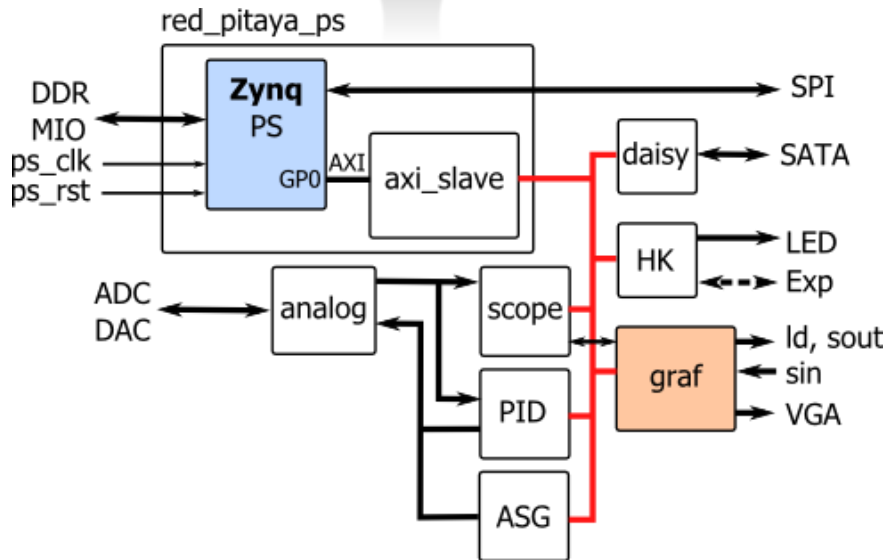
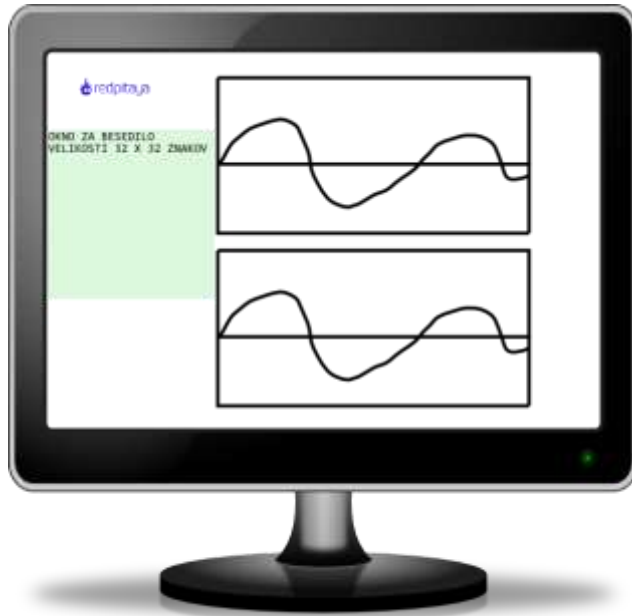


Senzorji	20,8 €
FPGA	10 €
Konektorji	3,5 €
R, C	3,4 €
OSC	3 €
TIV	2,9 €
V Reg	1,2 €
74HC, SPI	1,1 €





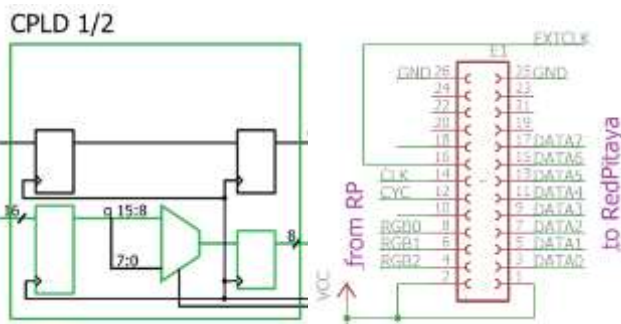
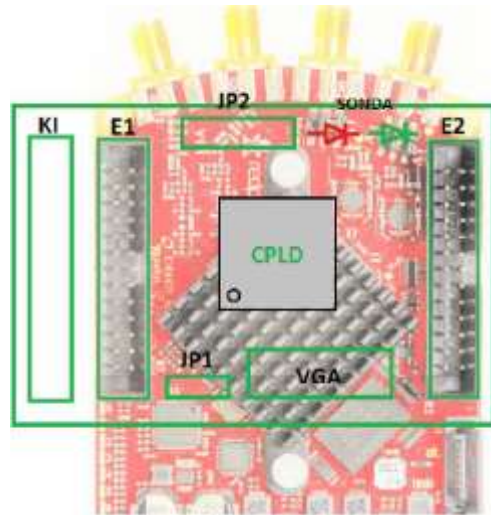
# Zajem in prikaz signalov na VGA





# Red Pitaya logični analizator (2015-16)

- ▶ vmesnik za zajem logičnih signalov (16 vhodov, proženje)
- ▶ grafični vmesnik (VGA)
- ▶ V/I za počasne signale (npr. tipke, LED...)





# Projekt 2016-17: digitalni osciloskop

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## 1. Logika

- ▶ orodja: VHDL simulator, Xilinx Vivado
- ▶ logika osciloskopa na Red Pitayi, testne strukture

## 2. Grafika

- ▶ orodja: VHDL simulator, Xilinx Vivado
- ▶ prikazovanje signalov in besedila

## 3. Vmesnik

- ▶ orodja: Eagle, VHDL simulator, Xilinx Vivado
- ▶ načrt tiskanega vezja in logika vmesnika v CPLD

## ▶ Skupne vaje

- ▶ logični gradniki in vmesniki (2x)
- ▶ osnovna shema vezja v programu Eagle (2x)
- ▶ sinhronizacija in prikaz VGA slike
- ▶ spajkanje in testiranje vezja

# Cilji, izvajanje in ocenjevanje DES 2016/17

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Študent bo znal:	Potek dela:	Ocenjevanje:
razložiti modeliranje digitalnih sistemov	predavanja, demonstracija	ustno
uporabiti ustrezne metode razvoja vezij	laboratorijske vaje	ocena vaj
opisati zasnovo in izvedbo digit. sistema	lab. projekt, skupinsko delo	ocena poročila
ovrednotiti različne tehnološke izvedbe	predavanja, diskusija	ustno
narediti RTL opis za izbrano nalogo	predavanja, vaje	ustno, reševanje na list